## INSTRUCTION TO CANDIDATES :

1. SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.
2. SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.
3. SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.

## SECTION-A

Q1. Answer briefly :
a. Convert binary number 100001111 into equivalent gray number.
b. Write excitation tables of SR and JK flip flops.
c. Compare CMOs with ECL
d. What are excess 3 codes? Where are they used?
e. Show that XOR gate acts as 1 bit comparator.
f. What is open collector logic?
g. What are De-Morgan theorems?
h. Compare PLA and PAL.
i. What are shift registers? What are their applications?
j. Determine conversion time of ADC for 8 -bit resolution at 2 MHz .

## SECTION-B

Q2. Implement the function $f(A, B, C, D, E)=\sum \mathrm{m}(0,3,5,8,9,15,18,31)$ using QM Method.
Q3. Explain the working of weighted resistor $\mathrm{A} / \mathrm{D}$ converter.
Q4. Design 4 bit Binary to Gray converter.
Q5. Convert D flip flop into JK flip flop.
Q6. Write note on accuracy and resolution of ADC.

## SECTION-C

Q7. Design a Mod 6 up down counter.
Q8. Explain the following :
a. Counter type ADC
b. Memory organization

Q9. Design a $B C D$ to seven segment decoder.

