Roll No. | | | | | | | | | | | | | Total No. of Pages : 02

Total No. of Questions : 09

B.Tech.(ECE)/(ETE) (2011 Onwards) (Sem.–6)

VLSI DESIGN

Subject Code : BTEC-604

Paper ID : [A2318]

Time : 3 Hrs. Max. Marks : 60

INSTRUCTION TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1. Answer briefly :

a. What are main feature of structural modelling in VHDL language?

b. What is the function of bus hold logic?

c. What do you mean by operator overloading in VHDL?

d. Define the term entity and architecture.

e. How simulation of sequential circuit is done?

f. What is noise margin in CMOS?

g. Differentiate between NMOS and PMOS.

h. What is sub threshold voltage?

i. Write VHDL code for NAND gate.

j. Differentiate between signal and variable.

SECTION-B

2. Describe package body with an example.

3. With an example, differentiate between data flow, behavioural circuit modelling.

4. Write the VHDL code for encoder.

5. Write VHDL code for full subtractor using half subtractor.

6. What is NMOS inverter? Discuss the transfer characteristics of it.

SECTION-C

7. Design and write VHDL code for 3- bit asynchronous up counter using D flip flop.

8. What is body effect? Discuss the MOS device equations.

9. Realize the following expression using NAND gate and Write VHDL code for it.

   F(A,B,C) = A'C'+ AB'C'+ABC+AB'C