Roll No. ☐☐☐☐☐☐☐☐☐☐☐☐   **Total No. of Pages : 02**

Total No. of Questions : 09

B.Tech.(ECE/ETE) (E-I 2011 Onwards)   (Sem.–6)
MICRO ELECTRONICS
Subject Code : BTEC-902
Paper ID : [A2390]

Time : 3 Hrs.   **Max. Marks : 60**

INSTRUCTION TO CANDIDATES :
1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

Q1. Answer briefly :

a. Write down the various specifications for ion Implantation method.

b. How fick's second law is derived from fick's first law?

c. Define gattering.

d. Write down the reaction for etching of silicon.

e. What do you mean by proximity effect?

f. Write down the names of various IC technologies.

g. Name the various impurities used in diffusion process.

h. With the help of table write down the various diffusion constants in SiO2 at 1100°C.

i. Calculate the RC time constant for a 1cm long doped polysilicon interconnection runner on 1 micro meter thick SiO2.the polysilicon has thickness of 5000°A and resistivity of $1000\mu\Omega$-cm.

j. Is it possible to design inductor on Ic technology? If not Why?

SECTION-B

Q2. Discuss feature size control and anisotropic etch mechanism.

Q3. What do you mean by electron lithography? What is the difference between raster and vector scan in electron lithography?

Q4. Discuss in detail about Gaussian diffusion.

Q5. What do you mean by annealing? Discuss various annealing techniques in detail.

Q6. Discuss the various short channel effects.

SECTION-C

Q7. What are the various steps used for CMOS IC technology?

Q8. Discuss the various chip testing techniques in detail.

Q9. What is the stored charge and the number of electrons on an MOS capacitor with an area of 4 μm^2, a dielectric of 200 Å thick SiO_2, and an applied voltage of 5V?