Roll No. ☐☐☐☐☐☐☐☐☐☐☐   **Total No. of Pages : 02**

Total No. of Questions : 09

B.Tech.(Automation & Robotics) (DE-I 2011 & Onward)
B.Tech.(ECE/ ETE) (E-I 2011 Onwards)
(Sem.–6)
DIGITAL SYSTEM DESIGN
Subject Code : BTEC-904
Paper ID : [A2392]

Time : 3 Hrs.   **Max. Marks : 60**

INSTRUCTION TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1.   **Answer briefly :**

   (a) What is function of a PLD?

   (b) List some applications of multiplexers.

   (c) Compare ROM and PROM.

   (d) What is FPGA?

   (e) What is PAL?

   (f) What do you mean by a Moore machine?

   (g) What is a ripple counter?

   (h) What do you mean by race-free state assignment?

   (i) List out the different methods by which a ROM can be programmed.

   (j) What is the operation of JK flip-flop?

SECTION-B

2. Explain various types of Read-Only-Memory (ROM).

3. What are the various methodologies of FPGA? Explain the same with neat diagram.

4. Explain the rules for clocking in FSM (finite state machine) design.

5. Design a BCD counter using appropriate programmable logic elements or device.

6. What are the key parameters to be considered while designing a logic circuit?

SECTION-C

7. Prove that two-level AND-OR circuit corresponding to the complete sum of a logic function is always hazard-free.

8. Draw the simplified block diagram of any Xilinx series FPGAs and discuss it.

9. Design a clocked synchronous state machine that checks a serial data line for even parity. The circuit should have two inputs, SYNC and DATA, in addition to CLOCK, and one Moore-type output, ERROR. Devise a state/output table that does the job using just four states.