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Total No. of Questions: 09

## B.Tech (ECE) (Sem.-7) <br> VLSI <br> Subject Code : EC-406 <br> Paper ID: [A0330]

Time : 3 Hrs.
Max. Marks : 60

## INSTRUCTIONS TO CANDIDATES :

1. SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.
2. SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.
3. SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.

## SECTION-A

1. Answer briefly :
a) What is Subprogram? Discuss the types of subprograms available in VHDL.
b) Differentiate between combinational \& sequential circuits with examples.
c) Explain the advantages of using FPGAs in IC design.
d) Describe the Logical \& arithmetic operators in VHDL.
e) Discuss the format of Concurrent statement with example.
f) Explain the concurrent assertion statement in VHDL.
g) Enumerate the difference between Data objects \& Data Types.
h) What are different specifications for the design of digital systems?
i) Differentiate between microcomputer and main frame computer.
j) What are the advantages of PLDs?

## SECTION-B

2. Explain data flow, structural and behavioral modeling with suitable examples.
3. Give the Behavioral 1 model of 4 bit SISO right shift register.
4. Write the VHDL code for 4:1 MUX using structural modeling.
5. How a simple microcomputer works? Explain its implementation using VHDL.
6. Implement Half Subtractor using PLAs.

## SECTION-C

7. Write briefly :
a) With a neat block diagram, explain PLA.
b) Implement the functions, $\mathrm{f}(x, y, z)=\Sigma \mathrm{m}(1,2,3,7)$ and $\mathrm{f} 2(x, y, z)=\Sigma \mathrm{m}(0,1,2,6)$ using PLA.
8. Write a short note on :
a) Generics
b) Operators in VHDL
c) Difference between CPLD \& FPGA
9. Write a VHDL code in structural style of modeling for SOP for the following expression:

$$
\mathrm{F}=\Sigma \mathrm{m}(1,4,6,8,9,11,12,14,15)+\Sigma \mathrm{d}(2,5,7)
$$

