Roll No. | | | | | | | | | | | | | Total No. of Pages : 02

Total No. of Questions : 09

B.Tech.(Electronics & Computer Engg.) (2011 Onwards) (Sem.–7,8)

VLSI DESIGN

Subject Code : BTEC-604

Paper ID : [A3244]

Time : 3 Hrs. Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

1. SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.
2. SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.
3. SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.

SECTION-A

1. Write briefly :

a. What do you understand by an entity? Give example.

b. What are three levels of architecture description?

c. What are concurrent statements?

d. What is meant by instantiating a component?

e. What do you mean by (a) latch (b) gated latch?

f. What is body effect in MOS?

g. Draw NMOS inverter.

h. What is power dissipation in MOS?

i. Distinguish between combinational and sequential circuits.

j. What are the effects of scaling on circuit performance?

SECTION-B

2. What is logical equivalent of CASE and IF-ELSE statements? Write one example using CASE statement and IF-ELSE each.

3. Write the VHDL code for Binary to Gray code converter.

4. Design 00 to 99 up-down counter with VHDL language.

5. Explain the working of depletion mode of MOSFET.

6. Derive the expression for pull up and pull down ratios of NMOS.

SECTION-C

7. Write the VHDL code for following logical expression :

$$Y=\sum m(1,5,7,9,11,13,15)$$

8. Define scaling of MOS circuits. What are different types of scaling? How circuits performace is effected with device scaling?

9. Write note on :

   a. Operator overloading

   b. CMOS inverter delays