Roll No. | | | | | | | | | | | | |  Total No. of Pages : 02

Total No. of Questions : 09

B.Tech.(Electronics & Computer Engg.) (E-II 2011 Onwards) (Sem.–7,8)

# CMOS BASED DESIGN

Subject Code : BTEL-905

Paper ID : [A3247]

Time : 3 Hrs. Max. Marks : 60

INSTRUCTION TO CANDIDATES :

1. SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.
2. SECTION-B contains FIVE questions carrying FIVE marks each and students has to attempt any FOUR questions.
3. SECTION-C contains THREE questions carrying TEN marks each and students has to attempt any TWO questions.

## SECTION-A

**Q.1 Write briefly:**

a) Write a spice program to obtain output characteristics of CMOS inverter.

b) Enlist three types of capacitors for CMOS technology.

c) What are the steps used for physical design in ASIC design flow?

d) Derive the equation for capacitance of MOS transistor.

e) What are the parameters which are not shown by the stick diagram?

f) Write the steps followed in the design of an Integrated Circuit.

g) What are the advantages of computer simulation techniques?

h) Draw the flow chart for bottom up approach for design implementation.

i) What do you mean by self heating in Integrated Circuits?

j) Draw stick diagram of N-MOS inverter.

## SECTION-B

Q.2 What is the significance of BSIM models? Enlist its features.

Q.3 Discuss various types of capacitors compatible with CMOS technology.

Q.4 What do you mean by parasitic estimation? Explain.

Q.5 Write a short note on following :

(a) Logical Efforts of the gate

(b) Parasitic delay of Gate.

Q.6 Discuss the working of N-channel active resistor with its I-V characteristics and small signal model.

## SECTION-C

Q.7 Draw and explain the Analog IC design flow.

Q.8 What are the various lambda based rules for CMOS design? Explain.

Q.9 Draw and explain the flow process for n-well twin tub CMOS process.