Roll No. | | | | | | | | | | | | | Total No. of Pages : 02

Total No. of Questions : 09

B.Tech (ECE) (2011 Batch E-III) (Sem.–7,8)

COMPUTER ORGANIZATION AND ARCHITECTURE

Subject Code : BTEC-914

M.Code : 71814

Time : 3 Hrs. Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

1. SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.
2. SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.
3. SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.

SECTION-A

1. Answer briefly :

a) Explain the concept of MIPS.

b) What is the principle of working of Cache memory?

c) What is cache coherence?

d) What is multithreading?

e) What is microinstruction sequencing?

f) What is the meaning of Superscalar architecture?

g) What is the difference between instruction and machine cycle?

h) What is point-to Point interconnecting?

i) What is pipelining?

j) What do you mean by multi core organization?

SECTION-B

2. Explain the Flynn's classification of computers.

3. Explain the concepts of computer organization and architecture.

4. What are the elements of cache design? Explain.

5. Explain the organization of typical register based CPU.

6. Explain the concept of vector computation.

SECTION-C

7. Why vector processors are expensive? What are their advantages?

8. What are Multi-core Processors? What are the Hardware and Software Performance Issues? Discuss Intel x 86 Multi-core organizations.

9. Explain the Fetch-decode and execute cycles in detail.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.