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Total No. of Pages : 02

Total No. of Questions : 08

M.Tech.(ECE) (Sem.-1)
ELECTRONICS SYSTEM DESIGN
Subject Code : EC-502
Paper ID : [E0562]

Time : 3 Hrs.

Max. Marks : 100

INSTRUCTION TO CANDIDATES :

1. Attempt any FIVE questions out of EIGHT questions.
2. Each question carries TWENTY marks.

1. a. Design a combinational logic that accepts 4-bit binary input and provides 4-bit output (Y3, Y2, Y1, Y0). The output Y3, Y2, Y1, and Y0 becomes high when input number in decimal is square, even, odd, prime number respectively.
b. Design a 4-bit controlled 1's complement circuit. The circuit provides 1's complement of the input when control signal is high ($M = 1$) else the output is same as the input when control is low ($M=0$).
2. a. Design a JK flip-flop using D flip-flop.
b. What is hazard? Determine the possible hazard in the Boolean expression given by $Y = AC' + A'D$.
3. a. Design an 8-bit controlled 1-bit left shifter with the help of 2:1 multiplexors. The design should left shift the input when control is asserted.
b. Write down the different steps of state reductions. Illustrate the advantages of state reduction.
4. a. Design a synchronous 4-bit serial-in serial-out left/right shift register using D flip-flops with control (M).
b. Design a finite state machine (Mealy machine) that provides output '1' when 1010 sequence is detected. The overlapping is allowed while detecting the sequence.
5. a. Derive the Boolean expression of full-adder and full-subtractor. Implement these full-adder and full-subtractor using PLA.

- b. Compare a digital circuit when implemented using ROM, PLA and PAL on the basis of implementation area, configurability and ease of implementation.
- 6. Design a 4-bit synchronous and asynchronous counter and compare them on the basis of performance, area and complexity.
- 7.
 - a. Explain the need of tri-state buffers in the bus-oriented systems. With the help of neat diagram, explain different buses in the electronic systems.
 - b. Write short notes on electromagnetic interference and electromagnetic compatibility grounding and shielding of digital circuits.
- 8.
 - a. What are prime timing issues we considered in the static timing analysis of sequential digital circuit? How these issues can be addressed?
 - b. How two systems can be synchronized? Write down steps of designing the controller for synchronization of two systems.

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