Roll No. | | | | | | | | | | | | | Total No. of Pages : 01

Total No. of Questions : 08

M.Tech. (Microelectronics) (Sem.–1)

VLSI DESIGN & TESTING

Subject Code : ME-805

Paper ID : [E0963]

Time : 3 Hrs. Max. Marks : 100

INSTRUCTIONS TO CANDIDATES :

1. Attempt any FIVE questions out of EIGHT question.
2. Each question carries TWENTY marks.

Q1. Discuss about the timing analysis of combinational and sequential circuits in detail. (20)

Q2. a) Explain in brief about Charge Couple Devices with neat diagram. (10)

b) Describe the need of state diagram in sequential machine design. (10)

Q3. a) Write a brief note on Programmable Logic Array. (10)

b) Explain the architecture of Xilinx XC - 9500 with suitable diagram. (10)

Q4. Discuss about dataflow and behavioral modeling in VHDL by considering a suitable example. (20)

Q5. a) Discuss the user defined primitives in Verilog with example. (10)

b) Briefly discuss about advanced modeling concepts in Verilog. (10)

Q6. Discuss in detail about the design of RAM and SDR with neat sketch (20)

Q7. a) Explain the method to eliminate meta - stability single synchronizer. (10)

b) Describe briefly about the Complex PLD's. (10)

Q8. a) Write a brief note on XC 4000 family of programmable logic devices. (7)

b) With a neat sketch explain the structure of standard PLD's. (7)

c) Explain the task and functions of Verilog in detail. (6)