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Rol Tot Tim INST 1. 2.	I No. Total No. of Pages al No. of Questions : 08 M.Tech. (Emb sys) (2016 & Onwards) (Sem1) ADVANCED DIGITAL SYSTEM DESIGN Subject Code : MTED-102 Paper ID : [74131] ne : 3 Hrs. Max. Marks : TRUCTION TO CANDIDATES : Attempt any FIVE questions out of EIGHT questions. Each question carries TWENTY marks.	100
Q1	a) Solve the following :	
	i) $(854013)_{8}$ - $(725360)_{8}$ .	
	ii) -48-23 using 2's complement method.	
	$iii)(1256)_{16} + (3DFF)_{16}$	(6)
	<ul> <li>b) Reduce the following function using k-map and realize using NAND gate and gate.</li> <li>E = ∑m(1,2,2,6,8,0,14,17,24,26,27,20,21) + ∑d(4,5).</li> </ul>	NOR (14)
00	$F = \sum m(1,2,3,0,8,9,14,17,24,20,27,30,31) + \sum m(4,3)$	(10)
Q2	a) Describe the various design steps of asynchronous machine.	(10)
	b) With the help of examples discuss the hazards in circuits developed by MEV meth	od. (10)
Q3	a) Write a procedure to add two n-bit vectors in VHDL.	(10)
	b) Develop a functional model for a full adder using selective signal assignment state	ement. (10)
Q4	Design a sequential circuit using D- flip flop with function as per the state diagram below.	shown

Fig.1

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Q5	a) Explain the D-algorithm with suitable example.	(10)
	b) What do you understand by built-in self test? Differentiate between exhaustive pseudo exhaustive testing.	re and (10)
Q6	a) Write a short note on packages and libraries.	
	b) What are generics? Explain the role of generics in VHDL with suitable example.	(10)
Q7	a) Discuss in detail about bridging fault model.	(10)
	b) Describe the algorithm steps involved in PODEM.	(10)
Q8	Implement the following using FPGA :	(20)
	a) 4:1 MUX	

b) 8×8 ROM

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