Roll No. | | | | | | | | | | | | | Total No. of Pages : 02

Total No. of Questions : 08

M.Tech. (EPDT) (2016 & Onwards) (Sem.–1)

ADVANCED DIGITAL SYSTEM DESIGN

Subject Code : MTET-102

Paper ID : [74136]

Time : 3 Hrs. Max. Marks : 100

INSTRUCTION TO CANDIDATES :

1. Attempt any FIVE questions out of EIGHT questions.
2. Each question carries TWENTY marks.

Q1 a. Convert the following hex numbers into its equivalent decimal number

i. 6B9H ii. 6D.3AH (6)

b. Perform the following : (6)

Convert to binary: $(19.75)_{10} = (\quad)_2$

Convert to octal: $(F4D2)_{16} = (\quad)_{10}$

c. What is difference between an unsigned and signed number? Explain with suitable examples. (8)

Q2 a. Implement the function $f = \sum m(0,2,3,4,6,7,8) + \phi(1,11,15)$ by using QM method. (8)

b. Draw the logic diagram to implement the Boolean equation using minimum number of logic gates (12)

$$Y = \left\{\left(\overline{A}.B.C\right)\left(A.\overline{B} + \overline{B} + \overline{C}\right)\right\} + C.\overline{D}$$

Q3 a. Simplify the following using K-map (10)

$$F(A,B,C,D) = CDE + \overline{A}B\overline{C}\,\overline{E} + \overline{A}BDE + \overline{A}BC\overline{E}$$

b. What is a binary cell? Design a binary cell mentioning all appropriate design steps. (10)

Q4 a. Describe various methods of converting a flow chart into MDS diagram with example. (10)

b. Design a circuit to convert RS flip-flop to JK flip-flop. (10)

Q5 a. Explain the design steps for traditional synchronous sequential circuits. (10)

b. Design a 3-bit, Mod-5 self correcting binary counter. (10)

Q6 a. Explain the design steps which can be used as logical design processes for development of asynchronous circuits (12)

b. What do you mean by FPGA? Discuss all the types of FPGA. (8)

Q7 a. Discuss various data types and logic operators available in VHDL. (10)

b. Write a VHDL code for Full Adder circuit. (10)

Q8 Write a note on : (20)

a. Faults in digital circuits.

b. Races and Cycles.

c. MEV approaches.