Roll No. | | | | | | | | | | | | |

Total No. of Pages : 01

Total No. of Questions : 08

M.Tech.(VLSI D) (2016 & Onwards) (Sem.–1)

HARDWARE DESCRIPTION LANGUAGES

Subject Code : MTVL-103

Paper ID : [74142]

Time : 3 Hrs. Max. Marks : 100

INSTRUCTION TO CANDIDATES :

1. Attempt any FIVE questions out of EIGHT questions.
2. Each question carries TWENTY marks.

1. a. Design a 4 bit Full adder using Generate Statement. (10)

   b. Explain Enumeration and Physical Data Type with example. (10)

2. Explain Operator Overloading and Subprogram Overloading with example. (20)

3. Write the code of string detector that takes as input a serial bit stream and outputs a '1' whenever the sequence "111" occurs. Overlap must be considered. (20)

4. a. Write VHDL code to implement Latch with a Guarded Block statement. (10)

   b. Explain Composite data type with examples. (10)

5. a. Write VHDL code for 2 input NOR gate with Rise/Fall time modeling using Generic Statement. (10)

   b. Design a 9-bit Parity Generator Circuit using Structural modelling. (10)

6. Define Attribute. Explain different types of Attribute in VHDL. (20)

7. Design a 3 bit up/down counter in behavioural and structure modeling using VHDL. (20)

8. Discuss on Configuration declaration and generics in Configuration in VHDL. (20)