Roll No. | | | | | | | | | | | | |

Total No. of Pages : 01

Total No. of Questions : 08

M.Tech.(VLSI D) (2016 & Onwards) (Sem.–1)

VLSI TECHNOLOGY

Subject Code : MTVL-104

Paper ID : [74143]

Time : 3 Hrs. Max. Marks : 100

INSTRUCTION TO CANDIDATES :

1. **Attempt any FIVE questions out of EIGHT questions.**
2. **Each question carries TWENTY marks.**

Ql. Define the role of particle size on clean room. Write steps to remove organic films, heavy metals and particulates from Silicon wafers.

Q2. a) With the help of Fick's laws for the diffusion, find out the diffusion profile for constant source diffusion.

b) What is the need of Annealing after Ion-implantation process? What are the advantages of ion-implantation over diffusion process?

Q3. a) To grow 1 micron of SiO_2 on Silicon substrate, what is the total thickness of Silicon that will be consumed in Wet oxidation method?

b) Write the Photolithographic process steps in details. Define positive and negative photoresists.

Q4. Define Epitaxy. Explain the working of any epitaxial growth technique with suitable diagram.

Q5. Explain DC sputtering in detail. Compare DC and RF sputtering process.

Q6. How does the Reactive Ion Etching (RIE) differ from plasma etching? What are the parameters that affect RIE process?

Q7. What is the self-aligned MOS technology? Show all the fabrication steps that are needed for n-MOS fabrication.

Q8. Define the role of High k and low k dielectrics for ULSI.