

**Total No. of Pages : 02**

**Total No. of Questions : 08**

**M.Tech.(ECE) (2016 Batch) (Sem.-1)**

# ELECTRONICS SYSTEM DESIGN

**Subject Code : MTEC-101**

**Paper ID : [74146]**

**Time : 3 Hrs.**

**Max. Marks : 100**

**INSTRUCTIONS TO CANDIDATES :**

1. Attempt any FIVE questions in all.
2. Each question carry TWENTY marks.

- Q1   a. Design and implement half adder and full adder using NOR gates.
- b. Implement the following function with a multiplier with B, C and D are to be select lines

$$F(A,B,C,D) = \Sigma(0,1,3,4,8,9,15).$$

- Q2
  - a. Design a circuit to convert D flip-flop to JK flip-flop.
  - b. What is a binary cell? Design a binary cell mentioning all appropriate design steps.
- Q3
  - a. Explain the design steps for traditional synchronous sequential circuits
  - b. Draw a neat diagram of master slave J-K FF. Explain how race around condition can be avoided in M-S J-K FF.
- Q4
  - a. Explain the MEV approaches to Asynchronous system designs in details.
  - b. Discuss the capabilities and limitations of Finite State Machines (FSM).
- Q5
  - a. Discuss the design approach with programmable system controller
  - b. Design a four bit gray to binary code convertor. Implement it using suitable ROM. Draw the ROM table and logic diagram.

- Q6 a. A combinational logic is defined by functions

$$F_1(A,B,C)=\sum m(1,3,5,6,7)$$

$$F_2(A,B,C)=\sum m(0,2,4,7)$$

Implement the circuit with PLA.

- b. Draw and Explain the indirect addressed multiplexer/ROM configuration.

- Q7 a. Explain the concept of cycles and races with suitable examples.
- b. Why shift registers are required? Discuss the various operation modes of shift registers.
- Q8 Write a note on :
- a. Active high/Active low digital circuits.
- b. Tri-state Bus.
- c. Explain MDS diagram.

[www.FirstRanker.com](http://www.FirstRanker.com)