Roll No. | | | | | | | | | | | | | Total No. of Pages : 01

Total No. of Questions : 08

M.Tech (VLSI Design) (Sem.–1)

CAD OF DIGITAL SYSTEM (Elective – I)

Subject Code : MTVL-PE1A-18

Paper ID : [75207]

Time : 3 Hrs. Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

1. **Attempt any FIVE questions out of EIGHT questions.**
2. **Each question carries TWELVE marks.**

1. a) Explain the most important entities that can be optimized for a VLSI design problem.

   b) Explain behavioral, structural and physical domains using Gajski's Y-chart.

2. a) Explain the different ways of checking the correctness of an integrated circuit without actually fabricating it.

   b) Explain Dijkstra's shortest-path algorithm with a suitable example.

3. What is integer linear programming (ILP)? Why ILP is useful in CAD for VLSI? Explain ILP with a suitable example.

4. a) Explain and compare simulation based placement algorithms.

   b) Explain floor planning algorithms for mixed block and cell design.

5. a) Classify global routing algorithms and explain Maze routing algorithm.

   b) Compare Steiner min-max tree based algorithm and weighted Steiner tree based algorithm.

6. a) Explain algorithm for minimizing doglegs of single row routing problem.

   b) Explain constraint graph based routing algorithms of two-layer channel routing algorithms.

7. Classify three layer channel layer algorithms. Compare extended net merge channel router and hybrid HVH-VHV router. Also, explain HVH routing from HV solution.

8. Write short notes on the following (**ANY TWO**) :

   a) FPGA

   b) Line-probe algorithm

   c) General and channel pin assignment