Roll No. | | | | | | | | | | | | | Total No. of Pages : 1

Total No. of Questions : 08

M.Tech.(ECE) E-I (Sem.–2)

VLSI DESIGN

Subject Code : EC-511

Paper ID : [E0570]

Time : 3 Hrs. Max. Marks : 100

INSTRUCTIONS TO CANDIDATES :

1. **Attempt any FIVE questions in all, out of EIGHT questions.**
2. **Each question carries TWENTY marks.**

Q1 a) What are the methods to eliminate meta-stability single synchronizer and double synchronizer?

b) Differentiate between combinational and sequential circuits with suitable examples.

Q2 a) Discuss Charge Coupled Devices in detail with a suitable diagram.

b) Discuss about the design of ROM in detail.

Q3 Explain various Verilog HDL model abstraction levels.

Q4 a) Discuss about the dataflow modeling in VHDL by considering a suitable example.

b) Describe various data types used in VHDL language with two examples for each.

Q5 a) Explain the architecture of Xilinx Xc-9500 with suitable diagram.

b) Write a short note on :

i. Configurable Logic Block.

ii. Input/ Output Block.

Q6 a) Describe the various logic operators used in VHDL language with two examples for each.

b) Discuss about the behavioral modeling in VHDL by considering a suitable example.

Q7 a) Explain the modeling of combinational logic in Verilog.

b) Discuss in detail about the tasks and functions in Verilog.

Q8 Discuss in detail about the design of SRAM and DRAM.