Roll No. | | | | | | | | | | | | |

Total No. of Pages : 01

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M.Tech (CSE Engg.) Big Data (PIT) (Sem.–2)

ADVANCED COMPUTER ARCHITECTURE

Subject Code : CSB-205

Paper ID : [51089]

Time : 3 Hrs. Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

1.Attempt any FIVE questions out of EIGHT questions.

2.Each question carries TWELVE marks.

Q1. Discuss in detail, the differences between Hardwired control unit design and Micro programmed control unit design.

Q2. Explain the block placement methods used in Cache Memory Management techniques.

Q3. Explain the methodology and different parameters used for evaluating the performance of multicore processors.

Q4. What is parallel processing and instruction-level parallelism (ILP)? Explain, in detail various dependencies caused in ILP.

Q5. a) Differentiate between centralized shared memory multiprocessors and distributed memory multiprocessors.

b) What is multithreading? How do you define thread level parallelism? How spin locks be implemented using coherence mechanism?

Q6. a) What are the causes for high miss rates in cache organization? What are the six basic cache optimizations?

b) How architecture supports for protecting processes from each other via virtual memory?

Q7. a) What is a pipeline? What are data dependences and hazards? Explain in detail.

b) Differentiate between software verses hardware solutions for hazard detection.

Q8. Write short notes on :

a) OpenMP Directives.

b) Synchronization and Race conditions in Multithreading.