Roll No. | | | | | | | | | | | | | Total No. of Pages : 01

Total No. of Questions : 08

M.Tech.(VLSI D) (2016 & Onwards) (Sem.–2)

ALGORITHMS FOR VLSI DESIGN AUTOMATION

Subject Code : MTVL-201

Paper ID : [74258]

Time : 3 Hrs. Max. Marks : 100

INSTRUCTIONS TO CANDIDATES :

1. **Attempt any FIVE questions out of EIGHT questions.**
2. **Each question carries TWENTY marks.**

Q1 a) Is reduced binary decision diagram of any Boolean function is unique? Justify your answer.

b) What is need of the system partitioning? Explain the problem formulation of the system portioning.

Q2 a) The floorplan of the circuit is expressed by the Polish expression E = 12H34V56VHV.

i) Why it is a desirable property to restrict ourselves to only normalized Polish expression?

ii) Give slicing tree corresponding to the Polish expression *E*.

b) What is meant by the circuit placement? Explain the effect of poor placement in the chip area.

Q3 Consider a circuit layout obtained after the placement step, that is, all the circuit components are already designed. Discuss the different possible cases for which pin-assignment step can reduce the wiring congestion in the circuit.

Q4 Discuss the effect of the routing in the chip area in detail. Explain the Soukup's routing algorithm.

Q5 List out the Steiner tree based routing algorithms and discuss briefly each of them.

Q6 Write down the differences between global and detailed routing. Explain the topological method of detailed routing.

Q7 Discuss briefly the different switchbox routing algorithms. Comment on the complexity of each algorithm.

Q8 Draw and discuss the High level synthesis flow of the digital system.