Roll No. | | | | | | | | | | | | | Total No. of Pages : 03

Total No. of Questions : 08

M.Tech. (VLSI D) (2016 & Onwards) (Sem.–2)

TESTING AND FAULT TOLERANCE

Subject Code : MTVL-202

Paper ID : [74259]

Time : 3 Hrs. Max. Marks : 100

INSTRUCTIONS TO CANDIDATES :

1. **Attempt any FIVE questions out of EIGHT questions.**
2. **Each question carries TWENTY marks.**

Q1 Explain the following faults :

a) Stuck-Open

b) Transient fault

c) Stuck-Short fault

d) Untestable fault **(4×5=20)**

Q2 Explain fault dominance and checkpoint theorem. For the circuit as shown in Figure I:**(20)**

a) What is the number of all potential fault sites?

b) Derive the equivalence collapsed set. What is the collapse ratio?

c) Derive the dominance collapsed set. What is the collapse ratio?

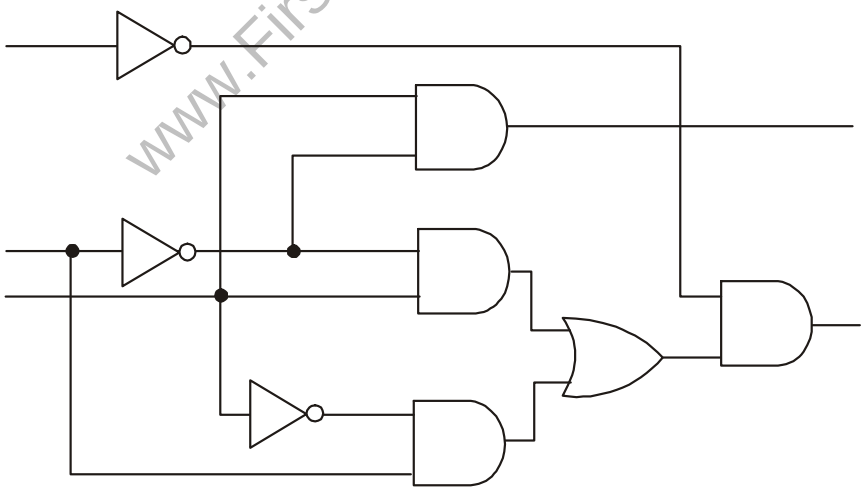

Figure 1 : Circuit diagram for problem 2.

Q3 a) Explain even-driven simulation with the help of suitable example. **(10)**

b) Assuming a four-bit machine word, demonstrate parallel fault simulation of vector (1,0.1) for the three single stuck-at-1 faults on the second primary input and its two fanouts, respectively, in the circuit of Figure 2. **(10)**

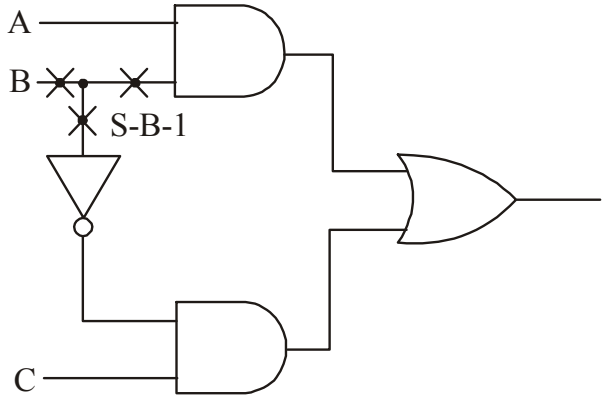

Figure 2 : Circuit for problem 3.

Q4 a) Explain different SCOAP controllability and observability metrics for combination circuits. **(10)**

b) Compute the SCOAP controllability and observability metrics for circuit given in Figure 3. **(10)**

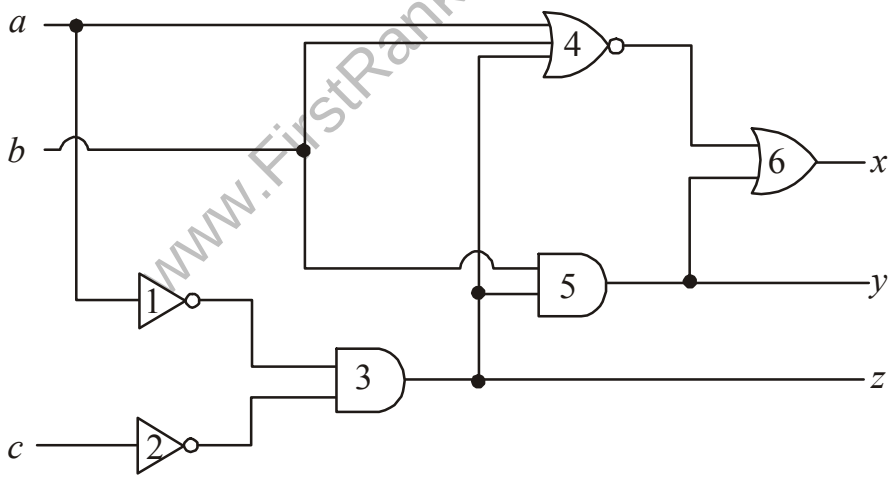

Figure 3 : Circuit for Problem 4.

Q5 a) Discuss path sensitization method of test pattern generation. **(10)**

b) Use Roth's D-ALG to perform ATPG for the sa l and for the sa 0 fault on the fanout branch h in the circuit shown in Figure 4 **(10)**

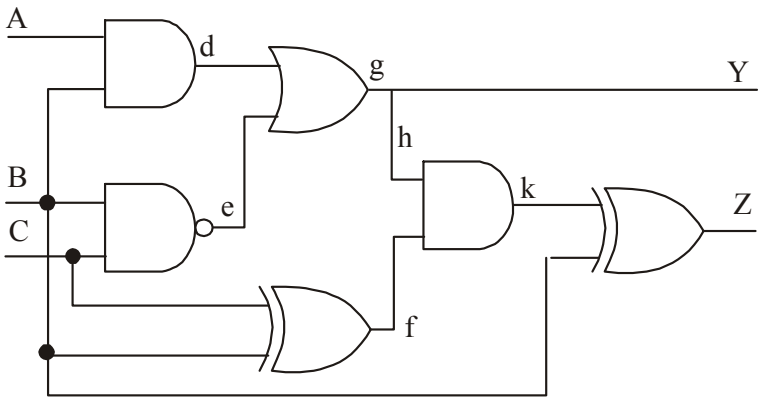

Figure 4: Circuit for Problem 5.

Q6 a) How do you perform generic boundary scan? **(10)**

b) Given two LFSR of polynomial $X^4 + X^3 + 1$ and $X^4 + X^2 + 1$ determine the m-sequence generated by LSB FFs with seed value '1000' and also compute the cycle length (LC) for both the LFSR.

Q7 a) Explain about TAP controller used in test-bus circuitry **(10)**

b) Draw the block diagram for a BIST implementation using BIBO and explain the test procedure. **(10)**

Q8 Write short notes on : **(4×5=20)**

a) Boundary scan standards

b) Error collection codes

c) Reconfiguration techniques

d) Yield modeling reliability