

Roll No.

Total No. of Pages : 02

Total No. of Questions : 08

M.Tech.(VLSI D) EL-II (2016 & Onwards) (Sem.-2)

LOW POWER VLSI DESIGN

Subject Code : MTVL-209

Paper ID : [74265]

Time : 3 Hrs.

Max. Marks : 100

INSTRUCTIONS TO CANDIDATES :

1. Attempt any FIVE questions out of EIGHT questions.
2. Each question carries TWENTY marks.

1. a) What are the different sources of power dissipation in digital CMOS circuit? Explain in detail. (10)
b) Explain the following :
 - i. Sub Threshold Swing.
 - ii. Effects of short channel length. (10)
2. a) Explain probabilistic power analysis techniques. (10)
b) Explain Monte-Carlo based technique for estimating the average power in sequential circuits. (10)
3. a) Use operation reduction technique to save area and power dissipation for the following operations : (6)
$$X^3 + AX^2 + BX + C$$

b) With suitable example show how the operation substitution technique helps in saving the power. (6)
c) Design different flip flops and latches circuits. Compare them with respect to performance and power perspective. (8)
4. What is Gate Reorganization? Explain different power saving techniques through Gate Reorganization, Signal gating, Logic encoding, State machine encoding and Precomputation logic. (20)

5. a) What is glitching power dissipation? How can it be minimized? (8)
b) How switching activity in sequential circuits is calculated? How switching activity can be reduced for low power digital systems? (12)
6. Explain power dissipation in clock distribution, signal driver vs. distributed buffers and zero skew vs. tolerable skew. (20)
7. a) Explain the design flow of architectural level methodologies. (10)
b) Explain algorithmic level analysis and optimization of algorithmic and architectural level methodologies. (10)
8. Write short notes on the following (**any two**) : (2×10=20)
 - a) Physics of power dissipation in CMOS devices.
 - b) Data correlation analysis in DSP systems.
 - c) Low power memory design.

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