Roll No. | | | | | | | | | | | | | Total No. of Pages : 01

Total No. of Questions : 08

M.Tech.(ECE) EL-I (2016 Batch) (Sem.–2)

VLSI DESIGN

Subject Code : MTEC-204B

Paper ID : [74282]

Time : 3 Hrs. Max. Marks : 100

INSTRUCTIONS TO CANDIDATES :

1. **Attempt any FIVE questions out of EIGHT questions.**
2. **Each question carries TWENTY marks.**

1. a) Discuss MTBF clocking strategies.
   b) What do you understand by SRAM? Explain its design with suitable diagrams.
2. Design a sequential circuit with two *J K* flip-flops A and B, and one input x. When x = 0, the state of the circuit remains the same. When x = l, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00, and repeats.
3. a) List the PAL programmable table the BCD-to-excess-3-code converter.
   b) Discuss programmable logic array (PLA) in detail with suitable diagram.
4. Explain configurable logic block and programmable routing matrix of Xilinx XC 4000 FPGA with the help of suitable diagrams.
5. a) Explain Hardware abstraction and basic terminology of VHDL language with suitable diagrams.
   b) If A = “01001”, B = “10011”, and C = “00010”, what are the values of the following statements?
      i) (A & B) or (B & C) ii) A rol 2
      iii) A sla 2 iv) A sra 3
6. a) Explain transport and inertial delays with example.
   b) Write VHDL code of a 4-bit BCD up counter using FSM approach. Also, write its test bench.
7. a) Design 4:16 decoder using two 3:8 decoders and write its code in Verilog HDL.
   b) What is a function? Write the code for finding greater of two signed numbers in Verilog using function.
8. Write short notes on the following (**any two**) :
   a) Mealy and Moore machines.
   b) FPGA.
   c) User defined primitives in Verilog.