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Roll No. | | | | | | | | | | | | | Total No. of Pages : 01

Total No. of Questions : 08

M.Tech (Embedded system) (Sem.–3)

SYSTEM ON CHIP

Subject Code : MTED-308

Paper ID : [74787]

Time : 3 Hrs. Max. Marks : 100

INSTRUCTIONS TO CANDIDATES :

1. **Attempt any FIVE questions out of EIGHT questions.**
2. **Each question carries TWENTY marks.**

1. a) Discuss the overview of the SOC design process.

   b) Explain the flow of SOC design Approach.

2. a) Explain the processor architecture and its implementation with neat sketch.

   b) Give overview of SOC external memory.

3. What are the basic cache organizations? Explain in detail. Also discuss split and multilevel chaches.

4. a) List the standard SOC buses. Explain AMBA buses.

   b) Explain the concept of PLB-processor local bus and OPB-on chip peripheral bus.

5. Explain system level, block level and hardware/ software co-verification process in detail.

6. a) Describe the Architecture of customizing instruction processor.

   b) Explain reconfigurable Interconnects.

7. a) Discuss the application study of image compression.

   b) Discuss the application study of AES algorithm.

8. Write short notes on the following (**ANY TWO**) :

   a) System architecture and complexity

   b) SOC memory system

   c) Antenna for SOC

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