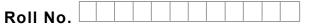


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M.Tech (VLSI Design) (Sem.-3) SYSTEM ON CHIP(SOC) Subject Code : MTVL-304 Paper ID : [74813]

Time : 3 Hrs.

Max. Marks: 100

INSTRUCTIONS TO CANDIDATES :

- 1. Attempt any FIVE questions out of EIGHT questions.
- 2. Each question carries TWENTY marks.
- Q1. a) Enlist five benefits and five challenges of timing driven design of system of Chip.
 - b) Draw the flow chart of SOC design flow and explain each step.
- Q2. a) Draw and explain the SOC memory model.
 - b) Draw and explain the Fully associative mapping in cache organization.
- Q3. a) What do you mean by "*cache miss*"? Which actions must be taken during "cache miss"? Explain.
 - b) What do you mean by bus bridge? What are the basic functions which are being served by bus bridge?
- Q4. a) Draw and explain a typical AMBA bus based system. Also, explain the goals achieved by AMBA bus design.
 - b) Enlist and explain what are the various system level issues and specifications for choosing a suitable interconnect architecture.
- Q5. a) What do you understand by network-on-chip approach for SOC? Explain with the help of diagram.
 - b) Describe advantages and disadvantages of On-Chip Buses.
- Q6. a) With the help of flow diagram, explain "Architecture Mapping".
 - b) Enlist and define at-least five important areas for Hardware/Software co-verification.
- Q7. In application view of SOC, explain AES with the help of Fully pipelined AES architecture diagram
- Q8. Write a short note on :
 - a) Cache organization
 - b) SOC peripheral cores
 - c) SOC memory system
 - d) Emulation

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