

**18ELN14/24**

**Visvesvaraya Technological University, Belagavi**

**MODEL QUESTION PAPER**

1<sup>st</sup> / 2<sup>nd</sup> Semester, B.E (CBCS)

**Course: 18ELN14/24- Basic Electronics – *Set no. 3***

**Note: (i) Answer five full questions selecting any one full question from each module.  
 (ii) Missing data may be suitably assumed**

**Time: 3 Hrs**

**Max. Marks: 100**

<b>MODULE 1</b>			
1	a	Explain the forward and reverse bias condition for a pn junction diode with neat diagram.	08M
	b	A half wave rectifier is fed from a supply of 230 V, 50 Hz with step down transformer of ratio 3:1. Resistive load connected is 10 K $\Omega$ . The diode forward resistance is 75 $\Omega$ and transformer secondary is 10 $\Omega$ . Calculate the DC load current, DC load voltage, efficiency and ripple factor.	06M
	c	Write a short note on the following: (i) Photo diode (ii) Light emitting diode.	06M
<b>OR</b>			
2	a	With neat circuit diagram and wave forms explain the working of a centre tapped full wave rectifier.	08M
	b	A Zener diode has a breakdown voltage of 10V. It is supplied from a voltage source varying between 20-40V in series with a resistance of 820 $\Omega$ . Using an ideal Zener model, obtain the minimum and maximum Zener currents	06M
	c	Explain the features of LM7805 fixed regulator.	06M
<b>MODULE 2</b>			
3	a	Explain the construction and operation of a p-channel JFET	08M
	b	With neat diagram explain the operation of a CMOS inverter.	06M
	c	With neat diagram explain the VI characteristics of an SCR.	06M
<b>OR</b>			
4	a	Explain the characteristics of an n-channel JEFT.	06M
	b	With neat diagram, explain the characteristics of a enhancement type MOSFET.	08M
	c	With neat diagram explain the two transistor model of an SCR.	06M

MODULE 3			
5	a	Explain the following with respect to op-amp (i) Input Impedance (ii) output impedance (iii) Slew rate (iv) CMRR (v) virtual ground	10M
	b	Derive an expression for the output voltage of an inverting amplifier.	06M
	c	The input to the basic differentiator circuit is a sinusoidal voltage of peak value of 10mV and frequency 1.5KHz. Find the output if, $R_f=100K\Omega$ and $C_1=1\mu F$ .	04M
OR			
6	a	Derive an expression for the output voltage of an op-amp integrator.	06M
	b	Derive an expression for the output voltage of an inverting summer.	06M
	c	A non-inverting amplifier circuit has an input resistance of $10K\Omega$ and feedback resistance $60K\Omega$ with load resistance of $47K\Omega$ . Draw the circuit. Calculate the output voltage, voltage gain, load current when the input voltage is 1.5V.	08M
MODULE 4			
7	a	Explain how the transistor can be used as a switch and as an amplifier.	10M
	b	An amplifier has a high frequency response described by $A = \frac{A_0}{1 + (j\omega/\omega_2)}$ . Where in $A_0=1000$ , $\omega_2=104$ rad/s. Find the feedback factor which will raise the upper corner frequency $\omega_2$ to 105 Hz. What is the corresponding gain of the amplifier? Find also the gain bandwidth product in this case.	04M
	c	With a neat circuit diagram, explain the working of RC phase shift oscillator.	06M
OR			
8	a	List the advantages of negative feedback in an amplifier. Explain the voltage series feedback amplifier. Show that the gain band width product for a feedback amplifier is constant.	10M
	b	The frequency sensitivity arms of the Wein bridge oscillator uses $C_1=C_2=0.01\mu F$ and $R_1=10K\Omega$ while $R_2$ is kept variable. The frequency is to be varied from 10KHz to 50 KHz by varying $R_2$ . Find the minimum and maximum values of $R_2$ .	04M
	c	With a neat diagram explain the Astable operation of IC 555 timer.	06M
MODULE 5			
9	a	Simplify the following Boolean expressions (i) $Y = A \bar{B} + AB$ (ii) $Y = AB + AC + BD + CD$ (iii) $Y = (B + CA)(C + \bar{A}B)$ (iv) $Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D$	08M
	b	With a neat circuit diagram and truth table, explain the working of a JK flip flop.	06M

	c	With a neat diagram, explain the working of a communication system.	06M
OR			
10	a	Simplify and realize the following using NAND gates only (i) $Y = AC + ABC + \bar{A}BC + AB + D$ (ii) $Y = A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B} + \bar{A}\bar{C}$	08M
	b	With a neat circuit diagram and truth table, explain the full adder circuit.	06M
	c	With a neat block diagram, explain the operating principle of the GSM system.	06M

[www.FirstRanker.com](http://www.FirstRanker.com)