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17CS34

(08 Marks)

## Third Semester B.E. Degree Examination, June/July 2019 Computer Organization

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

		ONE full question from each module.		
		Module-1		
cu GO",	1	<ul> <li>a. Write the basic performance equation. Explain the role of each of the parametequation of the performance of the computer.</li> <li>b. Draw and explain the connections between the processor and the main memory.</li> <li>c. Write a program to evaluate the arithmetic statement Y = (A + B) * (C + D) usin address, two-adderss, one—adderss and zero — address instructions.</li> </ul>	(04 Marks) (08 Marks)	
x 0.11 0.01 FG 11 , i, , i, , i,	2	OR a. What is an addressing mode? Explain any four addressing modes with examples. b. Explain the concept of stack frames, when subroutines are nested. c. Explain the shift and rotate operations with examples.	(08 Marks) (06 Marks) (06 Marks)	
6 17.' , = 0, 4g L., 4g 0 8	3 a	Module-2  . Give comparison between memory mapped I/O and I/O mapped I/O  b. Explain the following methods of handling interrupts from multiple devices.  i) Interrupt nesting /priority structure	(04 Marks)	
$\stackrel{O}{a}$ ) <sup>1=1</sup>		<ul><li>ii) Daisy chain method.</li><li>c. What is bus arbitration? Explain distributed arbitration with a neat diagram.</li></ul>	(08 Marks) (08 Marks)	
3 4 2 15 P;	4 &	OR  a. Draw neat timing diagrams and explain .  i) Multicycle synchronous bus transfer for a read operation.  Asynchronous bus transfer for a write operation.	(12 Marks)	
V 44 Z""-: ci ::21 E.;		<ul><li>b. Explain the following with respect to USB.</li><li>i) USB architecture</li><li>ii) USB addressing.</li></ul>	(08 Marks)	
wJ 0  '63'6.;Si E >> O -	5	Module-3 a. With a neat diagram, explain the internal organization of a 2M x 8 dynamic memory chip.  (08 Marks)		
		<ul><li>b. Distinguish between SRAM and DRAM.</li><li>C. Describe any two mapping functions in cache.</li></ul>	(04 Marks) (08 Marks)	
8 <b>Z</b>	6	OR a. What is virtual memory? With a diagram, explain how virtual memory address is translated?		
⊙ 5: , <del>,</del>		b. Define the following:  i) Memory latency ii) Memory bandwidth iii) Hit-rate iv) Miss-penalty	(08 Marks)	

Describe the working principle of a typical magnetic disk. www.FirstRanker.com