Code No: 07A3EC03 **R07** **Set No. 2**

II B.Tech I Semester Examinations,May 2011
SWITCHING THOERY AND LOGIC DESIGN
Common to BME, ICE, E.COMP.E, E.CONT.E, EIE, EEE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Differentiate between synchronous and asynchronous circuits.
   (b) Design a 2 to 4 decoder using NAND gates [8+8]

2. Draw an ASM chart for a synchronous sequential logic circuit which produces an output "THREE 1s" if three or more consecutive 1's follow the last 0 output. Design the data processing unit and a control unit for implementing the design. [16]

3. Explain the procedure for the following with an example
   (a) Conversion from Binary to decimal number
   (b) Binary subtraction using 1's complement
   (c) Binary subtraction using 2's complement
   (d) Conversion from gray to binary number [16]

4. (a) Design a 4-bit Bidirectional Shift Register.
   (b) Convert D flip flop to T flip flop. [8+8]

5. Convert the following Mealy machine into a corresponding Moore machine. [16]

PS	NS,Z	
	X=0	X=1
A	C,0	B,0
B	A,1	D,0
C	B,1	A,1
D	D,1	C,0

6. Design a combinational logic circuit with 4 inputs A, B, C, D. The output Y goes HIGH if and only if A and C inputs go HIGH. Draw the Truth table. Minimize the Boolean function using K-map. Draw the circuit diagram. [16]

7. Implement the following functions in a ROM. Specify the size of ROMs required to implement the following functions
   (a) Full adder
   (b) Binary to BCD converter [16]

8. (a) Convert the following SOP equation into its POS form.
   G = XY′Z + X′YZ′

(b) Reduce the following Boolean expressions to three literals.
A′C′ + ABC +AC′ 8+8]

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Code No: 07A3EC03 **R07** **Set No. 4**

II B.Tech I Semester Examinations,May 2011
SWITCHING THOERY AND LOGIC DESIGN
Common to BME, ICE, E.COMP.E, E.CONT.E, EIE, EEE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Draw an ASM chart for a synchronous sequential logic circuit which produces an output "THREE 1s" if three or more consecutive 1's follow the last 0 output. Design the data processing unit and a control unit for implementing the design. [16]

2. (a) Differentiate synchronous and asynchronous circuits
   (b) Design a 2 to 4 decoder using NAND gates [8+8]

3. Implement the following functions in a ROM. Specify the size of ROMs required to implement the following functions
   (a) Full adder
   (b) Binary to BCD converter [16]

4. Design a combinational logic circuit with 4 inputs A, B, C, D. The output Y goes HIGH if and only if A and C inputs go HIGH. Draw the Truth table. Minimize the Boolean function using K-map. Draw the circuit diagram. [16]

5. Convert the following Mealy machine into a corresponding Moore machine. [16]

PS	NS,Z	
	X=0	X=1
A	C,0	B,0
B	A,1	D,0
C	B,1	A,1
D	D,1	C,0

6. Explain the procedure for the following with an example
   (a) Conversion from Binary to decimal number
   (b) Binary subtraction using 1's complement
   (c) Binary subtraction using 2's complement
   (d) Conversion from gray to binary number [16]

7. (a) Design a 4-bit Bidirectional Shift Register.
   (b) Convert D flip flop to T flip flop. [8+8]

8. (a) Convert the following SOP equation into its POS form.
   G = XY′Z + X′YZ′

(b) Reduce the following Boolean expressions to three literals.
$A'C' + ABC + AC'$ 8+8]

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Code No: 07A3EC03 **R07** **Set No. 1**

II B.Tech I Semester Examinations,May 2011
SWITCHING THOERY AND LOGIC DESIGN
Common to BME, ICE, E.COMP.E, E.CONT.E, EIE, EEE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Design a combinational logic circuit with 4 inputs A, B, C, D. The output Y goes HIGH if and only if A and C inputs go HIGH. Draw the Truth table. Minimize the Boolean function using K-map. Draw the circuit diagram. [16]

2. (a) Convert the following SOP equation into its POS form.
   $G = XY'Z + X'YZ'$
   (b) Reduce the following Boolean expressions to three literals.
   $A'C' + ABC + AC'$ 8+8]

3. Explain the procedure for the following with an example
   (a) Conversion from Binary to decimal number
   (b) Binary subtraction using 1's complement
   (c) Binary subtraction using 2's complement
   (d) Conversion from gray to binary number [16]

4. (a) Differentiate synchronous and asynchronous circuits
   (b) Design a 2 to 4 decoder using NAND gates [8+8]

5. Convert the following Mealy machine into a corresponding Moore machine. [16]

PS	NS,Z	
	X=0	X=1
A	C,0	B,0
B	A,1	D,0
C	B,1	A,1
D	D,1	C,0

6. (a) Design a 4-bit Bidirectional Shift Register.
   (b) Convert D flip flop to T flip flop. [8+8]

7. Draw an ASM chart for a synchronous sequential logic circuit which produces an output "THREE 1s" if three or more consecutive 1's follow the last 0 output. Design the data processing unit and a control unit for implementing the design. [16]

8. Implement the following functions in a ROM. Specify the size of ROMs required to implement the following functions
   (a) Full adder

(b) Binary to BCD converter [16]

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Code No: 07A3EC03 **R07** **Set No. 3**

II B.Tech I Semester Examinations,May 2011
SWITCHING THOERY AND LOGIC DESIGN
Common to BME, ICE, E.COMP.E, E.CONT.E, EIE, EEE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Differentiate synchronous and asynchronous circuits
   (b) Design a 2 to 4 decoder using NAND gates [8+8]

2. Draw an ASM chart for a synchronous sequential logic circuit which produces an output "THREE 1s" if three or more consecutive 1's follow the last 0 output. Design the data processing unit and a control unit for implementing the design. [16]

3. Explain the procedure for the following with an example
   (a) Conversion from Binary to decimal number
   (b) Binary subtraction using 1's complement
   (c) Binary subtraction using 2's complement
   (d) Conversion from gray to binary number [16]

4. Convert the following Mealy machine into a corresponding Moore machine. [16]

PS	NS,Z	
	X=0	X=1
A	C,0	B,0
B	A,1	D,0
C	B,1	A,1
D	D,1	C,0

5. (a) Design a 4-bit Bidirectional Shift Register.
   (b) Convert D flip flop to T flip flop. [8+8]

6. Implement the following functions in a ROM. Specify the size of ROMs required to implement the following functions
   (a) Full adder
   (b) Binary to BCD converter [16]

7. Design a combinational logic circuit with 4 inputs A, B, C, D. The output Y goes HIGH if and only if A and C inputs go HIGH. Draw the Truth table. Minimize the Boolean function using K-map. Draw the circuit diagram. [16]

8. (a) Convert the following SOP equation into its POS form.
   $G = XY'Z + X'YZ'$

(b) Reduce the following Boolean expressions to three literals.
$A'C' + ABC + AC'$ 8+8]

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