Code No: 07A3EC16

R07

Set No. 2

II B.Tech I Semester Examinations, May 2011 DIGITAL LOGIC DESIGN

Common to Information Technology, Computer Science And Engineering, Computer Science And Systems Engineering

Time: 3 hours Max Marks: 80

Answer any FIVE Questions All Questions carry equal marks

- 1. Explain about the two ways to achieve a BCD Counter using a Counter with Parallel Load? [16]
- 2. (a) Design a circuit with four inputs and one output where the output is 1 if the input is divisible by 3 or 7.
 - (b) A safe has 5 locks:v,w,x,y,all of which must be unlocked for the safe to open. The keys to the locks are distributed among five executives in the following manner: Mr.A has keys for locks v& x

Mr.B has keys for locks v& y

Mr.C has keys for locks w& y

Mr.D has keys for locks x& z

Mr.E has keys for locks v& z

- i. Determine the minimal no. of executives required to open the safe.
- ii. Find all the combinations of executives that can open the safe, write an expression f(A,B,C,D,E) which specifies when the safe can be opened as a function of which executives are present
- iii. Who is the 'essential executive' without whom the safe cannot be opened.

[7+9]

- 3. Explain about the following:
 - (a) Merger diagrams
 - (b) Flow and implication tables.

[16]

- 4. (a) Implement Half adder using 4 NAND gates.
 - (b) Implement full subtractor using NAND gates only.

[6+10]

- 5. (a) design a 2 bit comparator using gates.
 - (b) Use an 8-to-1 MUX to design the following combinational logic circuit There are four adjacent parking slots in the XYZ Inc executive parking area. Each slot is equipped with a special sensor whose output is asserted high when a car is occupying the slot. Design a decoding system that will signal the existence of two or more adjacent vacant slots. [10+6]

Set No. 2

6. Tabulate the truth table for an 8 X 4 ROM that implements the Boolean functions

$$\begin{array}{l} A(x,y,z) = \sum (1,2,4,6) \\ B(x,y,z) = \sum (0,1,6,7) \\ C(x,y,z) = \sum (2,6) \\ D(x,y,z) = \sum (1,2,3,5,7) \end{array}$$

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Considering now the ROM as a memory, specify the memory contents at addresses 1 and 4? [16]

- 7. (a) What is the gray code equivalent of the Hex Number 3A7
 - (b) Find the biquinary of number code for the decimal numbers from 0 to 9
 - (c) Find 9's complement $(25.639)_{10}$
 - (d) Find (72532 03250) using 9's complement.

[4+4+4+4]

8. Explain about HDL for Sequential Circuits in Detail?

|16

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R07

Set No. 4

II B.Tech I Semester Examinations, May 2011 DIGITAL LOGIC DESIGN

Common to Information Technology, Computer Science And Engineering, Computer Science And Systems Engineering

Time: 3 hours Max Marks: 80

Answer any FIVE Questions All Questions carry equal marks

1. Explain about HDL for Sequential Circuits in Detail?

[16]

- 2. (a) Implement Half adder using 4 NAND gates.
 - (b) Implement full subtractor using NAND gates only.

[6+10]

- 3. Explain about the two ways to achieve a BCD Counter using a Counter with Parallel Load?
- 4. (a) What is the gray code equivalent of the Hex Number 3A7
 - (b) Find the biquinary of number code for the decimal numbers from 0 to 9
 - (c) Find 9's complement $(25.639)_{10}$
 - (d) Find (72532 03250) using 9's complement.

[4+4+4+4]

- 5. Explain about the following:
 - (a) Merger diagrams
 - (b) Flow and implication tables.

[16]

- 6. (a) design a 2 bit comparator using gates.
 - (b) Use an 8-to-1 MUX to design the following combinational logic circuit There are four adjacent parking slots in the XYZ Inc executive parking area. Each slot is equipped with a special sensor whose output is asserted high when a car is occupying the slot. Design a decoding system that will signal the existence of two or more adjacent vacant slots. [10+6]
- 7. Tabulate the truth table for an 8 X 4 ROM that implements the Boolean functions

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 $D(x,y,z) = \sum (1,2,3,5,7)$

Considering now the ROM as a memory, specify the memory contents at addresses 1 and 4?

8. (a) Design a circuit with four inputs and one output where the output is 1 if the input is divisible by 3 or 7.

Set No. 4

(b) A safe has 5 locks:v,w,x,y,all of which must be unlocked for the safe to open. The keys to the locks are distributed among five executives in the following manner: Mr.A has keys for locks v& x

Mr.B has keys for locks v& y

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Mr.C has keys for locks w& y

Mr.D has keys for locks x& z

Mr.E has keys for locks v& z

- i. Determine the minimal no. of executives required to open the safe.
- ii. Find all the combinations of executives that can open the safe, write an expression f(A,B,C,D,E) which specifies when the safe can be opened as a function of which executives are present
- iii. Who is the 'essential executive' without whom the safe cannot be opened.

 [7+9]

Set No. 1

II B.Tech I Semester Examinations, May 2011 DIGITAL LOGIC DESIGN

Common to Information Technology, Computer Science And Engineering, Computer Science And Systems Engineering

Time: 3 hours Max Marks: 80

Answer any FIVE Questions All Questions carry equal marks

- 1. Explain about the following:
 - (a) Merger diagrams

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(b) Flow and implication tables.

[16]

2. Tabulate the truth table for an 8 X 4 ROM that implements the Boolean functions

$$A(x,y,z) = \sum (1,2,4,6)$$

$$B(x,y,z) = \sum (0,1,6,7)$$

$$C(x,y,z) = \sum (2,6)$$

$$D(x,y,z) = \sum (1,2,3,5,7)$$

Considering now the ROM as a memory, specify the memory contents at addresses 1 and 4?

- 3. (a) Implement Half adder using 4 NAND gates.
 - (b) Implement full subtractor using NAND gates only.

[6+10]

- 4. (a) design a 2 bit comparator using gates.
 - (b) Use an 8-to-1 MUX to design the following combinational logic circuit There are four adjacent parking slots in the XYZ Inc executive parking area. Each slot is equipped with a special sensor whose output is asserted high when a car is occupying the slot. Design a decoding system that will signal the existence of two or more adjacent vacant slots. [10+6]
- 5. (a) Design a circuit with four inputs and one output where the output is 1 if the input is divisible by 3 or 7.
 - (b) A safe has 5 locks:v,w,x,y,all of which must be unlocked for the safe to open. The keys to the locks are distributed among five executives in the following manner: Mr.A has keys for locks v& x

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- i. Determine the minimal no. of executives required to open the safe.
- ii. Find all the combinations of executives that can open the safe, write an expression f(A,B,C,D,E) which specifies when the safe can be opened as a function of which executives are present

Set No. 1

iii. Who is the 'essential executive' without whom the safe cannot be opened. [7+9]

- 6. Explain about the two ways to achieve a BCD Counter using a Counter with Parallel Load? [16]
- 7. (a) What is the gray code equivalent of the Hex Number 3A7
 - (b) Find the biquinary of number code for the decimal numbers from 0 to 9
 - (c) Find 9's complement $(25.639)_{10}$

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(d) Find (72532 03250) using 9's complement.

[4+4+4+4]

8. Explain about HDL for Sequential Circuits in Detail?

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Set No. 3

II B.Tech I Semester Examinations, May 2011 DIGITAL LOGIC DESIGN

Common to Information Technology, Computer Science And Engineering, Computer Science And Systems Engineering

Time: 3 hours Max Marks: 80

Answer any FIVE Questions All Questions carry equal marks

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 - (b) Find the biquinary of number code for the decimal numbers from 0 to 9
 - (c) Find 9's complement $(25.639)_{10}$
 - (d) Find (72532 03250) using 9's complement.

[4+4+4+4]

- 2. Explain about the two ways to achieve a BCD Counter using a Counter with Parallel Load? [16]
- 3. Tabulate the truth table for an 8 X 4 ROM that implements the Boolean functions

 $A(x,y,z) = \sum (1,2,4,6)$

 $B(x,y,z) = \sum_{x} (0,1,6,7)$

 $C(x,y,z) = \sum (2,6)$

 $D(x,y,z) = \sum_{x} (1,2,3,5,7)$

Considering now the ROM as a memory, specify the memory contents at addresses 1 and 4? [16]

- 4. (a) Implement Half adder using 4 NAND gates.
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- 5. (a) Design a circuit with four inputs and one output where the output is 1 if the input is divisible by 3 or 7.
 - (b) A safe has 5 locks:v,w,x,y,all of which must be unlocked for the safe to open. The keys to the locks are distributed among five executives in the following manner: Mr.A has keys for locks v& x

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Mr.C has keys for locks w& y

Mr.D has keys for locks x& z

Mr.E has keys for locks v& z

- i. Determine the minimal no. of executives required to open the safe.
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- iii. Who is the 'essential executive' without whom the safe cannot be opened.

[7+9]

Set No. 3

6. Explain about the following:

Code No: 07A3EC16

- (a) Merger diagrams
- (b) Flow and implication tables.

[16]

7. Explain about HDL for Sequential Circuits in Detail?

[16]

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