Code No: 07A4EC09 **R07** **Set No. 2**

II B.Tech II Semester Examinations,APRIL 2011
SWITCHING THEORY AND LOGIC DESIGN
Common to Electronics And Telematics, Electronics And Communication Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Write the conversion procedures of the flip flops. Convert T flip flop to JK flip flop.
   (b) Convert SR flip flop to T flip flop. [8+8]

2. Consider the machine whose state table is given below.

PS	NS,Z	
	X = 0	X = 1
A	E,0	D,1
B	F,0	D,0
C	E,0	B,1
D	F,0	B,0
E	C,0	F,1
F	B,0	C,0

   Explain the state equivalence determination. When are the 2 states are distinguishable and when are the states are equivalent. [16]

3. (a) Implement the INVERTER gate, OR gate and AND gate using
      i. NAND gate
      ii. NOR gate
   (b) Define the gate which is used to compare the similarities in the input bits? Give the truth table and the logic symbol for that gate. [8+8]

4. Implement the following functions using 16:1 mux
   (a) F(w,x,y,z) = (w+x)(w′xy+yz)(xy′+w)
   (b) F(A,B,C,D) = (AB+C′D+B′D+ABC′) [16]

5. (a) Differentiate between i. Convert $(1596.675)_{10}$ hexadecimal
      ii. Convert $(11110.1011)_2$ to decimal
      iii. Convert $(10110001.01101001)_2$ to octal
      iv. Convert $(235.0657)_8$ to Binary
   (b) Obtain the 1's complement and 2's complement of the binary numbers
      i. 1011011
      ii. 0110101

iii. 10110
iv. 00110 [8+8]

6. Design a combinational logic circuit which performs the Binary multiplication that multiplies two 4-bit numbers. Use ROM to implement this design. [16]

7. Design a logic circuit with 4 inputs. The circuit should produce a 1 at its output when the excess-3 equivalent of the input consists of even number of 1's.Use K-map for minimization of the switching function. [16]

8. (a) Draw an ASM chart to implement the function of a SR flip flop.
   (b) Differentiate Conventional flow chart and Algorithmic state machine chart. [8+8]

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Code No: 07A4EC09 **R07** **Set No. 4**

II B.Tech II Semester Examinations,APRIL 2011
SWITCHING THEORY AND LOGIC DESIGN
Common to Electronics And Telematics, Electronics And Communication Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Design a combinational logic circuit which performs the Binary multiplication that multiplies two 4-bit numbers. Use ROM to implement this design. [16]

2. Design a logic circuit with 4 inputs. The circuit should produce a 1 at its output when the excess-3 equivalent of the input consists of even number of 1's.Use K-map for minimization of the switching function. [16]

3. (a) Implement the INVERTER gate, OR gate and AND gate using
   i. NAND gate
   ii. NOR gate
   (b) Define the gate which is used to compare the similarities in the input bits? Give the truth table and the logic symbol for that gate. [8+8]

4. (a) Draw an ASM chart to implement the function of a SR flip flop.
   (b) Differentiate Conventional flow chart and Algorithmic state machine chart. [8+8]

5. (a) Differentiate between i. Convert $(1596.675)_{10}$ hexadecimal
   ii. Convert $(11110.1011)_2$ to decimal
   iii. Convert $(10110001.01101001)_2$ to octal
   iv. Convert $(235.0657)_8$ to Binary
   (b) Obtain the 1's complement and 2's complement of the binary numbers
   i. 1011011
   ii. 0110101
   iii. 10110
   iv. 00110 [8+8]

6. Implement the following functions using 16:1 mux
   (a) F(w,x,y,z) = (w+x)(w′xy+yz)(xy′+w)
   (b) F(A,B,C,D) = (AB+C′D+B′D+ABC′) [16]

7. (a) Write the conversion procedures of the flip flops. Convert T flip flop to JK flip flop.
   (b) Convert SR flip flop to T flip flop. [8+8]

8. Consider the machine whose state table is given below.

PS	NS,Z	
	X = 0	X = 1
A	E,0	D,1
B	F,0	D,0
C	E,0	B,1
D	F,0	B,0
E	C,0	F,1
F	B,0	C,0

Explain the state equivalence determination. When are the 2 states are distinguishable and when are the states are equivalent. [16]

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Code No: 07A4EC09 **R07** **Set No. 1**

II B.Tech II Semester Examinations,APRIL 2011
SWITCHING THEORY AND LOGIC DESIGN
Common to Electronics And Telematics, Electronics And Communication Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Implement the INVERTER gate, OR gate and AND gate using
   i. NAND gate
   ii. NOR gate
   (b) Define the gate which is used to compare the similarities in the input bits? Give the truth table and the logic symbol for that gate. [8+8]
2. (a) Write the conversion procedures of the flip flops. Convert T flip flop to JK flip flop.
   (b) Convert SR flip flop to T flip flop. [8+8]
3. Design a combinational logic circuit which performs the Binary multiplication that multiplies two 4-bit numbers. Use ROM to implement this design. [16]
4. (a) Draw an ASM chart to implement the function of a SR flip flop.
   (b) Differentiate Conventional flow chart and Algorithmic state machine chart. [8+8]
5. Implement the following functions using 16:1 mux
   (a) F(w,x,y,z) = (w+x)(w′xy+yz)(xy′+w)
   (b) F(A,B,C,D) = (AB+C′D+B′D+ABC′) [16]
6. Consider the machine whose state table is given below.

PS	NS,Z	
	X = 0	X = 1
A	E,0	D,1
B	F,0	D,0
C	E,0	B,1
D	F,0	B,0
E	C,0	F,1
F	B,0	C,0

   Explain the state equivalence determination. When are the 2 states are distinguishable and when are the states are equivalent. [16]
7. (a) Differentiate between i. Convert $(1596.675)_{10}$ hexadecimal
   ii. Convert $(11110.1011)_2$ to decimal

iii. Convert $(10110001.01101001)_2$ to octal

iv. Convert $(235.0657)_8$ to Binary

(b) Obtain the 1's complement and 2's complement of the binary numbers

i. 1011011

ii. 0110101

iii. 10110

iv. 00110 [8+8]

8. Design a logic circuit with 4 inputs. The circuit should produce a 1 at its output when the excess-3 equivalent of the input consists of even number of 1's.Use K-map for minimization of the switching function. [16]

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Code No: 07A4EC09 **R07** **Set No. 3**

II B.Tech II Semester Examinations,APRIL 2011
SWITCHING THEORY AND LOGIC DESIGN
Common to Electronics And Telematics, Electronics And Communication Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Implement the INVERTER gate, OR gate and AND gate using
   i. NAND gate
   ii. NOR gate
   (b) Define the gate which is used to compare the similarities in the input bits? Give the truth table and the logic symbol for that gate. [8+8]

2. Consider the machine whose state table is given below.

PS	NS,Z	
	X = 0	X = 1
A	E,0	D,1
B	F,0	D,0
C	E,0	B,1
D	F,0	B,0
E	C,0	F,1
F	B,0	C,0

   Explain the state equivalence determination. When are the 2 states are distinguishable and when are the states are equivalent. [16]

3. Design a logic circuit with 4 inputs. The circuit should produce a 1 at its output when the excess-3 equivalent of the input consists of even number of 1's.Use K-map for minimization of the switching function. [16]

4. Design a combinational logic circuit which performs the Binary multiplication that multiplies two 4-bit numbers. Use ROM to implement this design. [16]

5. Implement the following functions using 16:1 mux
   (a) F(w,x,y,z) = (w+x)(w′xy+yz)(xy′+w)
   (b) F(A,B,C,D) = (AB+C′D+B′D+ABC′) [16]

6. (a) Write the conversion procedures of the flip flops. Convert T flip flop to JK flip flop.
   (b) Convert SR flip flop to T flip flop. [8+8]

7. (a) Differentiate between i. Convert $(1596.675)_{10}$ hexadecimal
   ii. Convert $(11110.1011)_2$ to decimal

iii. Convert $(10110001.01101001)_2$ to octal

iv. Convert $(235.0657)_8$ to Binary

(b) Obtain the 1's complement and 2's complement of the binary numbers

i. 1011011

ii. 0110101

iii. 10110

iv. 00110 [8+8]

8. (a) Draw an ASM chart to implement the function of a SR flip flop.

(b) Differentiate Conventional flow chart and Algorithmic state machine chart. [8+8]

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