Code No: 07A4EC13 **R07** **Set No. 2**

II B.Tech II Semester Examinations,APRIL 2011
COMPUTER ORGANIZATION
Common to IT, ICE, E.COMP.E, CSE, CSSE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain single precision and double precision calculations. In general how many bytes are used for both and what is the precision we get. Give some examples where double precision calculations are needed. [8]
   (b) Explain how we can identify arithmetic overflow has occurred or not while adding/subtracting two signed numbers. Draw the circuit for performing addition/substraction of two 4 bit numbers that checks the overflow. [8]

2. Explain the following with respect to serial communication:
   (a) Data Communication processor
   (b) Modem
   (c) Block Transfer
   (d) CRC
   (e) Full Duplex
   (f) Bit oriented protocol. [3+3+2+3+2+3]

3. (a) Draw the block diagram of a computer system and describe each of its parts along with their functions. Also designate the information flow between the parts with arrows. [5]
   (b) Explain the term memory bus bottleneck. [6]
   (c) Distinguish between multiprocessor and a multicomputer. [5]

4. (a) Support or oppose the statement. If we want to add a new machine language instruction to a processor instruction set, simply write a C program and compile and store the resultant code in control memory?. [8]
   (b) Support the statement Instruction Set Architecture has impact on the processors microarchitecture. [8]

5. Describe commonly employed bit shift operators such as shift left, right and arithmetic shift left/right. Design a circuit for register length of 4 bits using D Flip-Flops. [16]

6. What are the different types of Mapping Techniques used in the usage of Cache Memory? Explain. [16]

7. (a) Differentiate RISC and CISC computers.
   (b) Expalin RISC pipelining. [8+8]

8. Explain the following:
   (a) Daisy chain
   (b) Parallel arbitration
   (c) Dynamic arbitration algorithms. [5+5+6]

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Code No: 07A4EC13 **R07** **Set No. 4**

II B.Tech II Semester Examinations,APRIL 2011
COMPUTER ORGANIZATION
Common to IT, ICE, E.COMP.E, CSE, CSSE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Explain the following:
   (a) Daisy chain
   (b) Parallel arbitration
   (c) Dynamic arbitration algorithms. [5+5+6]
2. Describe commonly employed bit shift operators such as shift left, right and arithmetic shift left/right. Design a circuit for register length of 4 bits using D Flip-Flops. [16]
3. (a) Differentiate RISC and CISC computers.
   (b) Expalin RISC pipelining. [8+8]
4. Explain the following with respect to serial communication:
   (a) Data Communication processor
   (b) Modem
   (c) Block Transfer
   (d) CRC
   (e) Full Duplex
   (f) Bit oriented protocol. [3+3+2+3+2+3]
5. (a) Draw the block diagram of a computer system and describe each of its parts along with their functions. Also designate the information flow between the parts with arrows. [5]
   (b) Explain the term memory bus bottleneck. [6]
   (c) Distinguish between multiprocessor and a multicomputer. [5]
6. What are the different types of Mapping Techniques used in the usage of Cache Memory? Explain. [16]
7. (a) Support or oppose the statement. If we want to add a new machine language instruction to a processor instruction set, simply write a C program and compile and store the resultant code in control memory?. [8]
   (b) Support the statement Instruction Set Architecture has impact on the processors microarchitecture. [8]

8. (a) Explain single precision and double precision calculations. In general how many bytes are used for both and what is the precision we get. Give some examples where double precision calculations are needed. [8]

   (b) Explain how we can identify arithmetic overflow has occurred or not while adding/subtracting two signed numbers. Draw the circuit for performing addition/substraction of two 4 bit numbers that checks the overflow. [8]

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Code No: 07A4EC13 **R07** **Set No. 1**

II B.Tech II Semester Examinations,APRIL 2011
COMPUTER ORGANIZATION
Common to IT, ICE, E.COMP.E, CSE, CSSE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Explain the following with respect to serial communication:
   (a) Data Communication processor
   (b) Modem
   (c) Block Transfer
   (d) CRC
   (e) Full Duplex
   (f) Bit oriented protocol. [3+3+2+3+2+3]
2. (a) Differentiate RISC and CISC computers.
   (b) Expalin RISC pipelining. [8+8]
3. Describe commonly employed bit shift operators such as shift left, right and arithmetic shift left/right. Design a circuit for register length of 4 bits using D Flip-Flops. [16]
4. What are the different types of Mapping Techniques used in the usage of Cache Memory? Explain. [16]
5. (a) Draw the block diagram of a computer system and describe each of its parts along with their functions. Also designate the information flow between the parts with arrows. [5]
   (b) Explain the term memory bus bottleneck. [6]
   (c) Distinguish between multiprocessor and a multicomputer. [5]
6. (a) Support or oppose the statement. If we want to add a new machine language instruction to a processor instruction set, simply write a C program and compile and store the resultant code in control memory?. [8]
   (b) Support the statement Instruction Set Architecture has impact on the processors microarchitecture. [8]
7. Explain the following:
   (a) Daisy chain
   (b) Parallel arbitration
   (c) Dynamic arbitration algorithms. [5+5+6]

Code No: 07A4EC13 **R07** **Set No. 1**

8. (a) Explain single precision and double precision calculations. In general how many bytes are used for both and what is the precision we get. Give some examples where double precision calculations are needed. [8]

   (b) Explain how we can identify arithmetic overflow has occurred or not while adding/subtracting two signed numbers. Draw the circuit for performing addition/substraction of two 4 bit numbers that checks the overflow. [8]

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Code No: 07A4EC13 **R07** **Set No. 3**

II B.Tech II Semester Examinations,APRIL 2011
COMPUTER ORGANIZATION
Common to IT, ICE, E.COMP.E, CSE, CSSE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Describe commonly employed bit shift operators such as shift left, right and arithmetic shift left/right. Design a circuit for register length of 4 bits using D Flip-Flops. [16]

2. (a) Draw the block diagram of a computer system and describe each of its parts along with their functions. Also designate the information flow between the parts with arrows. [5]
   (b) Explain the term memory bus bottleneck. [6]
   (c) Distinguish between multiprocessor and a multicomputer. [5]

3. What are the different types of Mapping Techniques used in the usage of Cache Memory? Explain. [16]

4. Explain the following with respect to serial communication:
   (a) Data Communication processor
   (b) Modem
   (c) Block Transfer
   (d) CRC
   (e) Full Duplex
   (f) Bit oriented protocol. [3+3+2+3+2+3]

5. (a) Explain single precision and double precision calculations. In general how many bytes are used for both and what is the precision we get. Give some examples where double precision calculations are needed. [8]
   (b) Explain how we can identify arithmetic overflow has occurred or not while adding/subtracting two signed numbers. Draw the circuit for performing addition/substraction of two 4 bit numbers that checks the overflow. [8]

6. (a) Support or oppose the statement. If we want to add a new machine language instruction to a processor instruction set, simply write a C program and compile and store the resultant code in control memory?. [8]
   (b) Support the statement Instruction Set Architecture has impact on the processors microarchitecture. [8]

7. Explain the following:

(a) Daisy chain
(b) Parallel arbitration
(c) Dynamic arbitration algorithms. [5+5+6]

8. (a) Differentiate RISC and CISC computers.
(b) Expalin RISC pipelining. [8+8]

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