Code No: 07A50402 **R07** **Set No. 2**

III B.Tech I Semester Examinations,May 2011
LINEAR IC APPLICATIONS
Electronics And Communication Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Explain the performance parameters of a multiplier.
   (b) List the applications of multiplier. [8+8]
2. (a) Give the analysis of constant current bias circuit using zener diode.
   (b) For a differential amplifier, two sets of inputs are applied. The first set is $V_1 = 50\mu V$ and $V_2 = -50\mu V$ and the second set is $V_1 = 1050\mu V$ and $V_2 = 950\mu V$. If the CMRR is 100, calculate the percentage difference in the output voltage obtained for the two sets of the input signals. [8+8]
3. (a) List various advantages of IC technology over discrete component implementation.
   (b) Describe various technologies used to fabricate ICs. [8+8]
4. (a) Explain the operation of flash A/D converter.
   (b) Explain how dual slope A/D converter provides noise rejection.
   (c) If the maximum output voltage of a 7-bit D/A converter is 25.4V. What is the smallest change in the output as the binary count increases. [6+6+4]
5. (a) Draw the circuit and explain the operation of non-inverting amplifier with single supply.
   (b) Design a averaging amplifier circuit to provide a gain 5 for 4 input signals of same frequency. [8+8]
6. (a) Discuss the amplitude stabilization of phase shift oscillator.
   (b) Design an RC phase shift oscillator for 300 Hz frequency using IC 741 and$\pm$15 volt power supplies. Assume necessary component values. Suggest a method to reduce the output voltage swing to$\pm$6.5 volts [8+8]
7. (a) What is the meaning of voltage limiting? Show how it is obtained. [6]
   (b) Explain how to measure phase difference between two signals. [6]
   (c) What is Hysteresis? What parameters determine hysteresis. [4]
8. (a) Derive an expression for capture range of PLL.
   (b) Design a PLL circuit using 565 IC to get free running frequency = 4.5 KHz., lock range = 2 KHz.; Capture range = 100 Hz. Assume supply voltages of $\pm$10V are available. Show the circuit diagram. [8+8]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: 07A50402 **R07** **Set No. 4**

III B.Tech I Semester Examinations,May 2011
LINEAR IC APPLICATIONS
Electronics And Communication Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Explain the operation of RC phase shift oscillator using op-amp and derive the expression for frequency of oscillations.
   (b) List the merits and demerits of RC phase shift oscillator. [10+6]
2. (a) Using analog voltage divider circuit show that the output voltage is proportional to the division of the two analog inputs V1 and V2.
   (b) What are the modes of operation of a multiplier? Explain. [8+8]
3. (a) Obtain the frequency response of an op-amp using suitable mathematical expressions.
   (b) How fast can the output of an op-amp change by 10V if its slew rate is 1V / μS? [8+8]
4. (a) Derive the expression for the frequency of the output of an astable multivibrator.
   (b) A 555 timer is configured to run in astable mode with R1 = 20KΩ and R2 = 8KΩ and C = 0.1uf. Determine the output frequency and duty cycle. [10+6]
5. (a) What are the sources of errors in DAC? Explain.
   (b) The digital input for a 4-bit DAC is 0110 calculate its final output voltage.
   (c) Draw and explain the block diagram of IC 1408. [6+4+6]
6. (a) Draw the circuit diagram of a triangular wave generator using a comparator and integrator. Explain its operation by referring to the output waveform.
   (b) What is window detector? Explain its operation. [8+8]
7. (a) Distinguish between differential mode and common mode operations of differential amplifier.
   (b) For a dual input unbalanced output differential amplifier the various circuit parameters are $|V_{CC}| = |V_{EE}| = 10V$, $R_C = 4.7$ KΩ, $R_E = 6.8$ KΩ, $R_{S1} = R_{S2} = 50\Omega$, $\beta_{dc} = \beta_{ac} = 50$ and $V_{BE} = 0.7$V. find:
      i. Q point values
      ii. Voltage gain
      iii. Input resistance
      iv. Output resistance. [8+8]

Code No: 07A50402 **R07** **Set No. 4**

8. (a) What is an instrumentation amplifier? What are the basic requirements of a good instrumentation amplifier.

   (b) Design an instrumentation amplifier whose gain can be varied continuously over the range $1 \leq A \leq 1000$ use 100 kΩ potentiometer. [8+8]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: 07A50402 **R07** **Set No. 1**

III B.Tech I Semester Examinations,May 2011
LINEAR IC APPLICATIONS
Electronics And Communication Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Draw the circuit for converting a sinusoidal ware form into a square wave and into a series of pulses, one per cycle and explain.
   (b) Explain the operation of logarithmic multiplier with a circuit diagram. [8+8]
2. Carryout AC analysis of the differential amplifier using h-parameters and obtain the expressions for A_d, A_c, R_i and R_0 for dual input balanced output. [16]
3. (a) Explain how astable mode of 555 can be modified to get a square wave generator.
   (b) Design a 555 based square wave generator to produce a symmertrical square wave of 1 KHz. If V_{CC} = 12V. Draw the voltage across timing capacitor and the output. [8+8]
4. (a) Explain how a multiplier can be used as a voltage divider.
   (b) Describe square rooting circuit using multiplier. [8+8]
5. (a) Compare flash, dual slope and successive approximation register type ADCs.
   (b) Find out step size and analog output for 4-bit R-2R laddar DAC when input is 0100 and 1100. Assume V_{ref} = +5V. [8+8]
6. (a) Draw the circuit and explain the operation of instrumentation amplifier using transducer bridge. Derive the expression for its output voltage.
   (b) What are the applications of instrumentation amplifier? Explain. [10+6]
7. (a) Compare dominant pole and pole-zero compensation technique.
   (b) In the amplifier circuit shown in figure 1 $R_1 = 100\Omega$ R_f = 4.7 KΩ, CMRR = 90dB. If the amplitude of the induced 60 Hz noise at the output is 5V (rms) calculate the amplitude of the common mode input voltage V_{cm}.
8. (a) What is IGMF configuration? Explain.
   (b) Design a second order IGMF band pass filter with the following specification f_0 = 500 Hz. Gain at resonance = -5; bandwidth = 50 Hz. [8+8]

Code No: 07A50402 **R07** **Set No. 1**

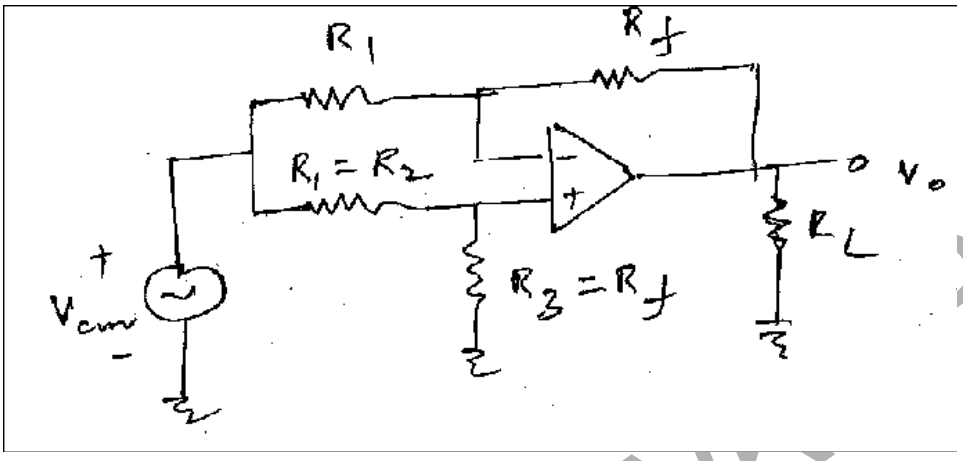

Figure 1

* * * * *

Code No: 07A50402 **R07** **Set No. 3**

III B.Tech I Semester Examinations,May 2011
LINEAR IC APPLICATIONS
Electronics And Communication Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Draw and explain the functional block diagram of IC 555.
   (b) Explain the functioning of 555 in Monostable configuration. [8+8]
2. (a) Describe parallel comparator type ADC operation.
   (b) For a Particular 8-bit ADC the conversion time is 9μS. find the maximum frequency of an input sine wave that can be digitized. 8+8]
3. (a) What is the name of the circuit that is used to detect the peak value of non-sinusoidal input wave forms? Explain its operation?
   (b) Distinguish between positive and -ve chipper circuits. Explain the operation of +ve and -ve chippers with the help of circuit and wave form. [8+8]
4. (a) Draw the basic circuit of wien bridge oscillator and explain its operation. Also derive the expression for frequency of oscillation.
   (b) Design the wien bridge oscillator circuit to have output frequency of 10 KHz. [8+8]

Code No: 07A50402 **R07** **Set No. 3**

5. (a) Discuss D.C. characteristics of op-amp in detail.

   (b) The input signal Vi to an op-amp is 0.04 Sin 1.13×10^5t is to be amplified to the maximum extent. How much maximum gain can be had by using op-amp, with slew rate of 0.4 V / Sec. [8+8]

6. (a) Draw the circuit and explain the operation of temperature compensated current source.

   (b) The specifications for the two stage cascaded differential amplifier are given below.

   First Stage: $R_{C1} = R_{C2} = 2.2K\Omega$; $R_{E1} = 4.7K$ Second Stage: RC3 = RC4 = 1.5 KΩ $R_{E2} = 1.5$ KΩ, $R_{E1} = 100\Omega$ The transistor specifications are h_{fe} = 10 h_{ie} = 1.47 KΩ and V_{BE} = 0.715 V, for all the transistors. The supply voltages are ± 10V, calculate:

   i. DC operating point values for both the stages
   ii. Overall differential voltage gain.
   iii. Output resistance
   iv. Input resistance.

   First stage is dual input balanced output stage, while the second stage output is single ended unbalanced. [8+8]

7. (a) Discuss the futures of balanced modulator IC 1496.

   (b) Explain the principle of operation of sample and hold circuit. [8+8]

8. (a) Explain how the averaging circuit can be derived from the summer.

   (b) Show that the output of the subtractor is proportional to the difference between the two input voltages.

   (c) Design the op-amp circuit which can give the output as $V_0 = 2\ V_1 - 3\ V_2 + 4V_3 - 5V_4$ [6+6+4]

⋆ ⋆ ⋆ ⋆ ⋆