Code No: 07A50403 **R07** **Set No. 2**

III B.Tech I Semester Examinations,May 2011
DIGITAL IC APPLICATIONS
Electronics And Communication Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Pertaining to VHDL, using schematies explain about Multiple processes and post poned processes. [16]

2. (a) What is metastability experienced in operation of a D latch?
   (b) Explain how metastability problem of D latch is eliminated in an edge triggered D flip-flop?
   (c) Write a VHDL program to simulate the behavior of a positive edge triggered D flip-flop. [6+5+5]

3. (a) Differentiate between logic comparator and a magnitude comparator. Discuss the two types in view of implementation.
   (b) Design a comparator circuit which compares two 4-bit logic vectors and indicates whether both of them are same or not. Produce an active low output Z to assert the equality condition. [8+8]

4. (a) Draw the truth table and circuit diagram of a 2-to-4 decoder with an additional control signal to decide the polarity of the outputs of the decoder.
   (b) Describe how the decoder designed above can be implemented in an 8x4 Read Only Memory.
   (c) Reason out if the realization of a 2-to-4 decoder in 8x4 ROM has only one implementation possibility. [5+5+6]

5. (a) Write data flow VHDL program for 4-bit prime number detector.
   (b) Discuss about simulation of a VHDL code. Take the VHDL program of 5(a) as example. [8+8]

6. Draw the typical Input-Output & transfer characteristics of CMOS Inverter and explain about the various terms associated with the characteristics. Explain the term Noise Margin. [16]

7. Draw the TTL NAND gate and CMOS NAND gate circuit and explain their operation. Compare the performance of these logic gates in all respects. [16]

8. Write the VHDL code for simulating an 8x8 combinational multiplier in behavioral model explaining the steps of multiplication as comments in the code. [16]

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Code No: 07A50403 **R07** **Set No. 4**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) Write general syntaxes for Entity and Architectures.
   (b) Expalin about structural design elements. [8+8]
2. (a) How many address and data lines are required to access all the locations of Dynamic RAM cell arrays specified below.
   i) 4M x 4
   ii) 1M x 1
   iii) 1M x 4
   iv) 4M x 1
   (b) Differentiate between an SRAM and a DRAM. [8+8]
3. (a) Describe how a number represented in single precision floating point can be converted into a corresponding binary number.
   (b) What are the advantages of representing integers/numbers in floating point format?
   (c) Design a 4-bit magnitude comparator to produce equal to and not equal to as the output conditions. [6+5+5]
4. Draw the function table and write the corresponding VHDL code with necessary select lines to simulate a 4-bit ALU to perform the following logical and arithmetical functions. F = A OR B, F = A XOR B, F = assign 1111 to B, F = NOT (A) OR B, F = A MINUS B, F = A PLUS B PLUS CIN, F = (A MINUS B) MINUS 1, F = (A PLUS B) PLUS 1, F = (A PLUS B) PLUS (CIN MINUS 1). [16]
5. Using waveforms and sketches, explain about Inertial Delay model and Transport Delay model for VHDL. [16]
6. (a) Explain the operation of a master-slave SR flip flop through its internal functional-timing diagram.
   (b) Comment on the predictability of Q and Q' outputs of master-slave flip-flop when both S and R inputs become high at the same time when rising edge of clock signal occurs.
   (c) Discuss about the predictability of outputs in the case of a JK flip-flop configured in master-slave structure. [16]
7. Draw the circuit for CMOS AND gate, its functional table and symbol and explain its working clearly. [16]

8. Draw the circuits for TTL, CML and CMOS OR logic gates and explain their working. Compare their characteristics in all respects. [16]

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Code No: 07A50403 **R07** **Set No. 1**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. What are the different styles of writing VHDL programs, explain them. [16]
2. How many groups of Data types are there in VHDL? Giving examples for each type explain about them. [16]
3. (a) Construct a full adder circuit using two half adders and basic logic gates.
   (b) Draw the circuit diagram of a 4-bit ripple carry adder using 4 full adder circuit blocks.
   (c) Compare and contrast ripple carry adder and a carry-look-ahead adder for same number of input bits. [6+5+5]
4. (a) Discuss the requirement of representing and performing arithmetic operations on integers/numbers in floating point format.
   (b) Write a VHDL program to simulate a 6-bit magnitude comparator to produce 6 outputs listed as, 'A = B', 'A $\neq$B' , 'A < B', 'A < B', 'A > B' and 'A > B'. [8+8]
5. Explain how MOSFET device can be used as logic element? Draw the CMOS Inverter circuit and explain its functioning. [16]
6. (a) Draw the circuit diagram and function table of a positive edge triggered commercial D flip-flop which is similar to one of the two flip-flops on an MSI IC 74x74.
   (b) What is a scan flip-flop? Draw the extra logic necessary to convert a normal flip-flop into a scan flip flop. Draw its function table and logic symbol. [8+8]
7. (a) List various types of Read only memories commercially available. Briefly describe the functionalities and capabilities of each of these commercial ROMs.
   (b) With the help of suitable block diagram, explain how a digital attenuator is realized in a ROM for μ-law companding to PCM encode speech signals. [8+8]
8. Draw the circuit for Diode logic AND gate and explain its operation with the help of truth table. compare this logic family with TTL and CMOS logic family. [16]

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Code No: 07A50403 **R07** **Set No. 3**

III B.Tech I Semester Examinations,May 2011
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Draw the circuit diagram of an edge triggered D-type flip-flop with preset' and 'clear' control signals.
   (b) With the help of the function table of a D-flip flop, explain the operation of a positive edge triggered D-flip flop.
   (c) With the help of suitable circuit diagram explain how scan chain of D flip flops is used to test application Specific ICs (ASIC) [6+5+5]
2. What are the Relational operators and Equality operator? Give examples and explain about them. [16]
3. (a) Is a Read only memory, a sequential circuit? Substantiate your answer with the help of the internal diagram of a ROM.
   (b) Design a ROM to store the truth table of a 3-to-8 decoder combinational circuit. [8+8]
4. What is the use of packages and libraries in VHDL? Explain with examples. [16]
5. Draw the circuit for CMOS OR logic gate and explain its working clearly, giving truth table and symbol. [16]
6. (a) Describe the functionality of a 2 - to - 4 decoder and a 4-to-1 multiplexer in a 4-bit barrel shifter.
   (b) Write a VHDL code in structural model to simulate a 4-bit barrel shifter.[8+8]
7. Explain how CMOS-TTL interfacing can be achieved. Give the input and output levels of voltages and explain the same. [16]
8. (a) Write VHDL code in dataflow model to implement the function of MSI chip 74X138, a 3-to-8 decoder with active high outputs and three enable inputs G_1, G2A and G2B. G1 is active high while G2A and G2B are active low enable signals. The outputs should be enabled only when all the three enable units are asserted.
   (b) Rewrite the VHDL code for the 74× 138 type 3-to-8 decoder specified above in behavioral model using process statement. Write the truth table for the circuit simulated. [8+8]

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