Code No: 07A50504 **R07** **Set No. 2**

III B.Tech I Semester Examinations,May 2011
MICROPROCESSORS AND INTERFACING
Common to Information Technology, Instrumentation And Control Engineering, Electronics And Computer Engineering, Computer Science And Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Why do we prefer interrupt driven data transfer than programmed I/O transfer? Show the complete hardware design to resolve the multiple interrupts based on priority? [16]

2. (a) Explain task switching operation in 80386?
   (b) What are the features of RISC over CISC? [8+8]

3. (a) Draw the block diagram of 8279 and explain each block?
   (b) Explain different modes of operation of 8255 and how they are initialized in control word? [8+8]

4. It is necessary to serve 15 interrupt requests using 8259's. The address map for the 8259's is given from 0100H to 0103H. Show the complete interface with 8086 system bus? These 15 interrupts are to be requested from interrupt type 060H on words, with level trigged mode and auto end of interrupt. Give the initialization sequence for all 8259's. [16]

5. Discuss the following signal descriptions?
   (a) ALE/PROG
   (b) $\overline{EA}$ / V_{PP}
   (c) $\overline{PSEN}$
   (d) RXD
   (e) $\overline{INT_0}$ / $\overline{INT_1}$
   (f) TXD
   (g) T_0 AND T_1
   (h) $\overline{RD}$ [16]

6. (a) Explain in detail the coding template for 8086 MOV instruction?
   (b) Write briefly about
      i. PUBLIC directive
      ii. EXTERN directive [8+8]

7. (a) Explain USB operation?

(b) Interface 8251 with 8086 at address 0A010H. Initialize it in asynchronous mode, with 6 bit character size, baud rate factor 16, one start bit, two stop bits, odd parity enable? [8+8]

8. It is necessary to check the parity of the data byte in location 2000H:01FEH. If the parity is even store 00H otherwise store 0FFH in location 8000H:1000H. Give the instruction sequence for every addressing mode to achieve the above result.[16]

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Code No: 07A50504 **R07** **Set No. 4**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) Explain the instruction support of 8051 to read data from lookup tables stored in EPROM?
   (b) Explain the counter/timer operation of 8051? Explain how this can provide clock for baud rate setting in serial data transmission through 8051? [8+8]
2. (a) Explain the real address mode operation of 80386 and show how physical address is generated?
   (b) Bring out the architectural differences between 80386 and Pentium processor. [8+8]
3. (a) Write a sequence of instructions to communicate to a modem using 8251 at address 080H.
   (b) Give the specifications of
      i. RS-232C
      ii. RS-423A [8+8]
4. Write an initialization sequence for an 8259 that is the only 8259 in an 8086 based system, with an even address of 0040H that will cause.
   (a) Request to the level triggered mode
   (b) IR_0 request to an interrupt type 28
   (c) SP/EN to output a disable signal to the data-bus transceivers.
   (d) The ISR bits to be cleared automatically at the end of second INTA pulse.
   (e) The IMR to be cleared.
   (f) The highest priority interrupt will be IR_3. [16]
5. (a) Discuss various branch instruction of 8086 microprocessor, that are useful for relocation?
   (b) Using a do-while construct, develop a sequence of 8086 instructions that reads a character string from the keyboard and after pressing the enter key the character string is to be displayed again. [8+8]
6. 8086 processor do not provide memory indirect addressing mode. Show all possible ways to access a word from memory where the segment address is given in location C000H:1000H and the offset is given in location C000H:1002H. Give the instruction sequence for every addressing mode of 8086.? [16]

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7. (a) Draw the block diagram of 8279 and explain the functionality?
   (b) Design a counter type ADC using 8255? Make necessary assumptions and give the software listing? [8+8]

8. What is function of ready pin in 8086. Draw the circuit diagram for wait state generation between 0 and 7 wait status and draw the corresponding timing diagram. [16]

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Code No: 07A50504 **R07** **Set No. 1**

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1. (a) Discuss the serial data transmission standards and their specifications.
   (b) Explain the necessity of RS232 to TTL interface and draw the circuit.
   (c) Draw the circuit of TTL to RS232 and explain the necessity of this interface. [16]

2. (a) Draw the block diagram of 80386 and explain each block?
   (b) List out various privilege levels of 80286 and explain their functionality? [8+8]

3. The register contents of 8086 is given below. CS=5000H, DS=8000H, SS=A000H, ES=B000H, SI=2000H, DI=6000H, BP=1002H, SP=0002H, AX=0000H, BX=5200H, CX=2000H, DX=2000H Calculate the effective address and physical address of the following instructions.
   (a) IMUL AX, [BP+BX-8D]
   (b) SBB AL, ES:[SI+5D]
   (c) PUSH AX
   (d) AND AH, [SI+42D]
   (e) CMPSB
   (f) CMP DX, [SI]
   (g) XOR DH, [DI+8D]
   (h) DIV AX, [SI+2] [16]

4. (a) Using REPEAT-UNTIL construct, develop a sequence of 8086 instructions that reads a character string from the keyboard and after pressing the enter key the character string is to be displayed again.
   (b) What is a procedure? Give an example to declare a procedure as near? Make this procedure as PUBLIC procedure? [8+8]

5. Interface a stepper motor with 8-step input sequence to 8086 based system and write the instruction sequence to move the stepper motor 20 steps in clockwise and 12 steps in anti-clockwise direction. [16]

6. (a) What is the difference between HALT state and HOLD state? Discuss the status of different control pins of 8086 in both the states?

(b) What are the control signals useful for inter processor communication using 8086? What instruction set support is provided in 8086? [8+8]

7. With detailed hardware and the associated algorithm, explain how a real time clock will be implemented in an 8086 based system. [16]

8. An 8051 based system requires external memory of four 4Kbytes of SRAM each and two chips of EPROM of size 2Kbytes. The EPROM starts at address 2000H. SRAM address map follows EPROM map. Give the complete memory interface. [16]

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Code No: 07A50504 **R07** **Set No. 3**

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1. (a) What are the common flags in 8086 and 8085 processors? Discuss about each of the flags.
   (b) List out segmentation resisters of 8086? Explain how 8086 provides 1 MB memory address space using the segment registers? What is the purpose of extra segment. [8+8]

2. Draw and discuss the formats and bit definitions of the following SFRs in 8051 microcontroller?
   (a) IP
   (b) TMOD
   (c) TCON
   (d) SCON [16]

3. Explain the following data transfer schemes.
   (a) Programmed I/O
   (b) Interrupted I/O
   (c) DMA [16]

4. Develop an 8086 assembly language program that reads a key from the keyboard and converts it to uppercase before displaying it. The program needs to terminate on typing the 'Crtl + C' key combination. [16]

5. (a) Write an instruction sequence that will cause the priority of an 8259, whose even address is 0C00H, to be IR_5, IR_6, IR_7, IR_0, IR_1, IR_2, IR_3, IR_4. Solve this problem when the current priority is IR1 and for the second time assuming the current priority to be IR_7?
   (b) Explain with examples how interrupt type 1 and type 3 provide debugging feature? [8+8]

6. (a) 8255 is interfaced with 8086 processor with the address map of 8000H to 8003H. Give the hardware design?
   (b) Port A is configured in mode 2 with active interrupt. Give the instruction sequence for initialization? Provide the timing diagram of the handshake signals for the bi-directional data transfer? [8+8]

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7. (a) Explain the protected virtual address mode of 80386 and show how 24 bit physical address is generated?

   (b) Discuss the specific features of code and data cache of Pentium processor and also discuss the merits and demerits? [8+8]

8. (a) What are the MODEM control lines? Explain the function of each line? Discuss how MODEM is controlled using these lines with necessary sequence of instructions?

   (b) Interface 8251 with 8086 at address 0F0H. Initialize it in asynchronous mode, with 8 bit character size, baud rate factor 16, one start bit, two stop bits, even parity enable? [8+8]

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