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SET - 1

III B.TECH - I SEMESTER EXAMINATIONS - MAY, 2011 DIGITAL SIGNAL PROCESSING (COMMON TO BME, E.COMP.E)

Time: 3hours Max. Marks: 80

Answer any FIVE questions All Questions Carry Equal Marks

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- 1.a) Give the detailed block diagram of Digital signal Processing system and list out its advantages, limitations over analog signal processing.
 - b) Verify whether the following systems are linear, time invariant, and causal or not i) y(n) = anx(n) ii) y(n) = ax(n-1) + bx(n-2). [8+8]
- 2.a) Define DFT and IDFT. Compute the DFT of the given time domain sequence $x(n) = \{1,2,3,4,4,3,2,1\}.$
 - b) State and prove Linearity, Circular Time Shift and Circular Frequency shift properties of DFT. [8+8]
- 3.a) Compare the Computational complexity of DFT and FFT
 - b) Compute FFT of the given sequence $x(n) = \{8, 3, 5, 6, 7, 8, 4, 5\}$ using Radix-2 DIT FFT. [8+8]
- 4. Obtain Direct form-I, Direct form-II, Parallel and Cascade form realization of the given LTI system governed by the difference equation y(n) = -3/8 Y(n-1) + 3/32 y(n-2) + 1/64 y(n-3) + x(n) + 3 x(n-1) + 2 x(n-2). [16]
- 5.a) Compare and Contrast Bilinear & Impulse Invariant transformation technique.
 - b) Prove that the relationship between analog (Ω) and digital (ω) frequency in bilinear transformation is given by $\Omega = (2/T) \operatorname{Tan} (\omega/2)$. [8+8]
- 6.a) Compare various windowing techniques with respect to side lobes and beam width.
 - b) Design an FIR Digital High pass filter using Hamming window whose cutoff frequency is 1.2 rad/s and length of window N=9. [8+8]
- 7.a) What is the importance of Multirate Signal Processing and hence define Decimation and Interpolation.
 - b) Discuss the process of decimation with a neat block diagram and explain how the aliasing effect can be avoided. [8+8]
- 8.a) Discuss the internal architecture of a TMS 320C54xx Digital signal processor
 - b) Explain six stage pipeline architecture of TMS320C54xx processor. [8+8]

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SET - 2

III B.TECH - I SEMESTER EXAMINATIONS - MAY, 2011 DIGITAL SIGNAL PROCESSING (COMMON TO BME, E.COMP.E)

Time: 3hours Max. Marks: 80

Answer any FIVE questions All Questions Carry Equal Marks

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- 1.a) Define Linearity, Time invariant, Stability and Causality
 - b) Derive the BIBO stability condition for the given system to be stable. [8+8]
- 2.a) Define DFT and IDFT. Compute the IDFT of the given time domain sequence $x(n) = \{1,2,3,4,4,3,2,1\}.$
 - b) Bring out the relationship between DFS and Z- Transform. [8+8]
- 3. Derive the necessary expressions for computing FFT using DIF Algorithm and hence Compute FFT of the given sequence $x(n) = \{1,2,3,4,4,3,2,1\}$ using Radix-2 DIF FFT Algorithm. [16]
- 4.a) Define Z- Transform. Determine the unit step response for the systems given by the difference equation y(n) + 3y(n-1) + 2y(n-2) = 2x(n) x(n-1).
 - b) What is transposed form structure? Give the Direct form I and transposed structure for the given difference equation y(n) = 3x(n)+2x(n-1)+5x(n-3)-3y(n-1)-7y(n-3). [8+8]
- 5.a) Compare and Contrast Butterworth and Chebyshev approximations
 - b) Bring out the relation between analog and digital filter poles using Impulse Invariant transformation and hence bring out the relation between analog and digital frequency. [8+8]
- 6.a) Compare FIR and IIR filters.
- b) Design a High Pass FIR filter whose cut-off frequency is 1.2 radians/sec and N=9 using Hamming Window and draw the frequency response curve. [8+8]
- 7.a) Define Multirate Signal Processing. Discuss the process of Interpolation with a neat block diagram.
 - b) Explain the implementation of polyphase filter structure for interpolators. [8+8]
- 8.a) Discuss various data addressing modes of TMS320C54xx processors.
 - b) Explain VLIW architecture of Programmable DSP Processor. [8+8]

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SET - 3

III B.TECH - I SEMESTER EXAMINATIONS - MAY, 2011 DIGITAL SIGNAL PROCESSING (COMMON TO BME, E.COMP.E)

Time: 3hours Max. Marks: 80

Answer any FIVE questions All Questions Carry Equal Marks

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- 1.a) Discuss various discrete time sequences.
 - b) Determine the output sequence of the system with impulse response $h(n) = (1/2)^n$ when the input is the complex exponential sequence $x(n) = A.e^{j\pi n/2}$.

[8+8]

- 2.a) Find X(K) of the given time domain sequence $x(n) = \{1,2,3,4,5,6,7,8\}$
 - b) List out all the properties of DFT with necessary equations.

[8+8]

- 3. Develop DIF FFT algorithm for decomposing the DFT for N=12 by considering the factors N=3.4. [16]
- 4.a) What are the basic blocks of filter realization structures. Hence discuss Cascade and Parallel form of realization structures.
 - b) Obtain the cascade and parallel realization structures for the following signal $y(n) = \frac{3}{4}y(n-1) \frac{1}{8}y(n-2) + x(n) + \frac{1}{3}x(n-1)$. [8+8]
- 5.a) Compute the poles of an Analog Chebyshev filter TF that satisfies the Constraints

 $0.707 \le |H(j\Omega)| \le 1$; $0 \le \Omega \le 2$ $|H(j\Omega)| \le 0.1$; $\Omega \ge 4$ and determine Ha(s) and hence obtain H(z) using Optimum transformation.

- b) Discuss the frequency warping effect in realization of digital filters using Bilinear transformation method. [8+8]
- 6.a) Compare FIR and IIR filters.
 - b) Derive the necessary and sufficient condition for the FIR filter to be stable.[8+8]
- 7.a) What is the importance of Multirate Signal Processing in real time applications and hence discuss the Process of decimation with the help of necessary equations.
 - b) Explain the Design of Phase shifters with the help of a neat block diagram. [8+8]
- 8.a) Explain six stage pipeline architecture of TMS320C54xx processor.
 - b) Discuss various data addressing modes of TMS320C54xx processors. [8+8]

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SET - 4

III B.TECH - I SEMESTER EXAMINATIONS - MAY, 2011 DIGITAL SIGNAL PROCESSING (COMMON TO BME, E.COMP.E)

Time: 3hours Max. Marks: 80

Answer any FIVE questions All Questions Carry Equal Marks

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- 1.a) Write a short note on classification of systems.
 - b) Show that the output of an LTI system is given by the convolution of the input and output sequences. [8+8]
- 2.a) What is the importance of DFT and hence bring out the relation between Z-Transform and DFT.
 - b) Compute the convolution of two given sequences $x(n) = \{1 \ 2 \ 3 \ 4\}$ and $y(n) = \{4 \ 3 \ 2 \ 1\}$ using DFT. [8+8]
- 3. Develop DIT FFT algorithms for decomposing the DFT for N=6 and draw the flow diagrams for N = 2.3 and apply for the computation of DFT for $x(n) = \{1,2,3,4,5,6\}$. [16]
- 4.a) Define Z- Transform and List out the properties of Z- Transform.
 - b) Determine the parallel realizations of IIR digital filter transfer functions $H(Z) = 3 (Z^2+5Z+4) / (2Z+1)(Z+2)$. [8+8]
- 5.a) Explain the aliasing effect in realization of digital filters using Impulse invariant technique.
 - b) Convert the analog filter into a digital filter whose system function is $H(S) = (S+0.2) / (S+0.2)^2 + 9$ using impulse invariant technique. Assume T =0.5s [8+8]
- 6.a) Discuss various cases of frequency response of FIR filter design.
 - b) Compare various windowing techniques of FIR design with respect too side lobe and beam width. [8+8]
- 7.a) Define Decimation and Interpolation.
 - b) Discuss the sampling rate conversion by a factor I/D with necessary equations.

[8+8]

- 8.a) Discuss the internal architecture of a TMS 320C54xx Digital signal processor.
 - b) Discuss various data addressing modes of TMS320C54xx processors. [8+8]

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