

Code No: 07A51102

R07**Set No. 2**

III B.Tech I Semester Examinations, May 2011
LINEAR AND DIGITAL IC APPLICATIONS
Common to Bio-Medical Engineering, Electronics And Computer
Engineering, Electronics And Telematics, Electronics And Control
Engineering

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions
 All Questions carry equal marks

1. (a) What are the advantages of the adjustable voltage regulators over the fixed voltage regulators.
 (b) Differentiate between an integrator and a differentiator. [8+8]
2. List and explain any two applications of PLL in detail. [16]
3. (a) What is the need for a parity checker?
 (b) Design an odd parity generator, for an 8 bit binary words. [8+8]
4. (a) Design a first -order low pass filter so that it has a cut off frequency of 2kHz and pass Band gain of '1'
 (b) Convert the 2kHz low pass filter to a cut off frequency of 3kHz in part (a) [8+8]
5. Explain the features of the TTL logic family. [16]
6. Explain with neat block diagram a typical application in which A/D and D/A conversions are employed? [16]
7. What is the voltage at point A and B for the circuit as shown in figure 1 if $V_1 = 5V$ and $V_2 = 5.1V$. [16]

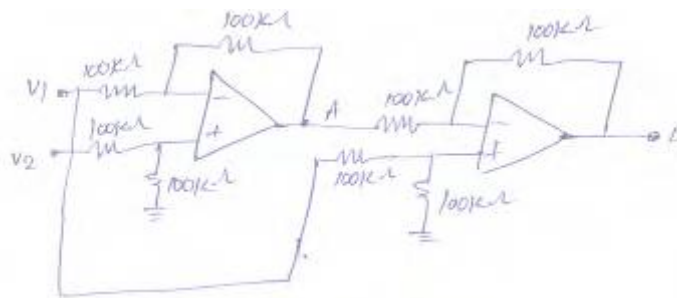


Figure 1:

8. (a) Explain how programming a RAM is different from programming a ROM?
 (b) Explain about DRAMs. [8+8]

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1. (a) How many bits are required to design a DAC, that has a resolution of 5mv? The ladder has +8V full scale.
 (b) How many resistors are required for an 8-bit weighted resistor DAC? What are the resistance values, assuming the smallest resistance is R? [16]
2. (a) Design a First order HPF at a cut off frequency of 3kHz.
 (b) Draw the frequency response of the above filter. [8+8]
3. (a) Explain Astable multivibrator as a square wave oscillator.
 (b) With a circuit explain 555 timer as a free running multivibrator. [8+8]
4. (a) Explain why open loop configurations are not used in linear applications?
 (b) For an op-Amp, PSRR=70dB(min), CMRR= 10^5 , differential mode gain $A_d=10^5$, The output voltage changes by 20v in 4 μ seconds. Calculate
 - i. Numerical value of PSRR
 - ii. CMRR
 - iii. Slew rate. [16]
5. Implement the following functions using a multiplexer.
 - (a) $F(A,B,C) = \sum m(1,3,5,6)$
 - (b) $F(A,B,C) = \sum m(0,1,3,4,8,9,15)$ [16]
6. Explain Static and dynamic RAM's, their characteristics, advantages, disadvantages, and applications. [16]
7. (a) Draw the wave forms of the comparator for $V_{ref} > 0$ and $V_{ref} < 0$.
 (b) For the strain gauge bridge circuit as shown in figure 2, given that $V_{ab} = -V_{dc} \left(\frac{\Delta R}{R} \right)$. Assume that under the strained conditions the resistances R_{T1} and R_{T3} decreases and that of R_{T2} and R_{T4} increases by the same amount $\Delta R \Omega$ Also $R_{T1} = R_{T2} = R_{T3} = R_{T4} = R$, under unstrained conditions. [4+12]
8. Explain the MOS and CMOS logic families and give different CMOS characteristics. [16]

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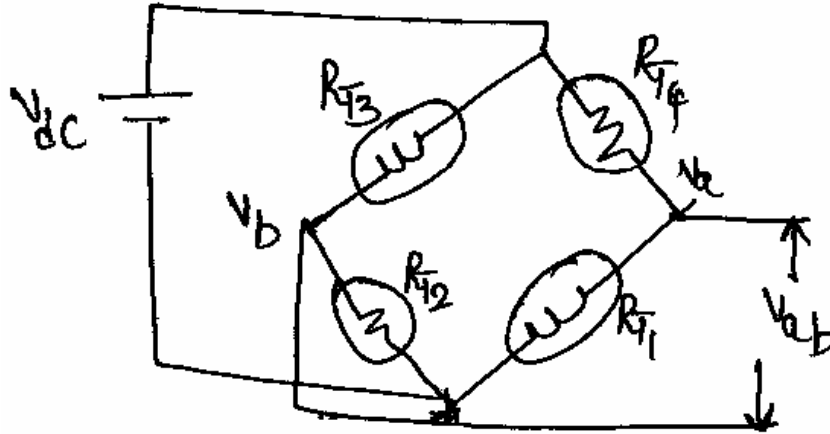


Figure 2

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1. (a) Explain the importance of 555 timer in designing a monostable multivibrator
 (b) Design a monostable multivibrator using 555 timer to produce a pulse width of 100msec. [16]
2. (a) Design a second order high pass filter at a cut off frequency of 1kHz.
 (b) Draw the frequency response of the network in part (a). [16]
3. (a) Write short notes on the following:
 - (i) Level triggering.
 - (ii) Edge triggering.
 - (iii) Pulse triggering.
 (b) Explain the functioning of RS flip-flop using NAND gates. [8+8]
4. (a) Explain the operation of a monostable multivibrator.
 (b) For the integrator circuit as shown in figure 3 the input is a sine wave with a peak-to-peak amplitude of 5V at 1kHz. Draw the output voltage waveform if $R_1 C_F = 0.1\text{ms}$ and $R_F = 10R_1$. Assume that the voltage across C_F is initially zero. [6+10]

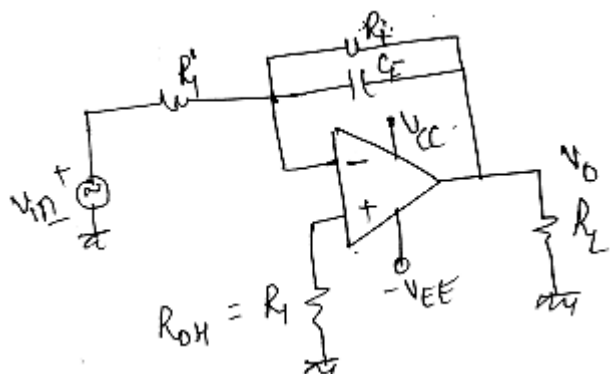


Figure 3

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5. (a) What are the sources of analog errors in an ADC?
 (b) What is meant by differential linearity an ADC? [8+8]
6. With the help of a neat circuit diagram explain how extremely low propagation in ECL logic can be achieved. [16]
7. Show that the input impedance for the non-inverting amplifier circuit as shown in figure 4 is $R_{if} = R_i \left(1 + \frac{z_1}{z_1 + z_f}\right) A_V$ where R_i the input impedance of OPAMP and $R_0=0$ and A_V is the gain without feedback. [16]

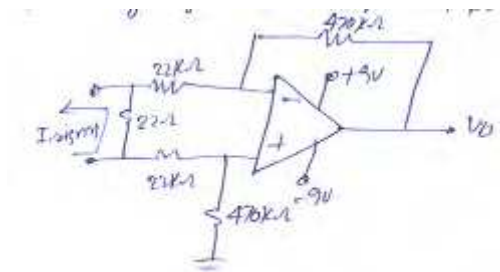


Figure 4:

8. (a) Explain parity generator and parity checker?
 (b) Design a digital comparator for 2-bit numbers? [8+8]

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1. (a) With neat circuit diagram explain a master-slave Flip-flop and also draw the timing diagram
 (b) Explain about asynchronous Flip Flops. [8+8]
2. (a) Explain the concept of current mirror circuit by drawing the circuit.
 (b) What is an integrated circuit chip? What it consist of? [8+8]
3. (a) Explain the current limiting feature of 723 regulator?
 (b) Design a differentiator that will differentiate an input signal with $f_{max}=100\text{Hz}$. [8+8]
4. For a second order butter worth filter given $C_2 = C_3 = 0.047\mu F$;
 $R_2 = R_3 = 3.3k\Omega$, $R_1 = 27k\Omega$, and $R_F = 15.8k\Omega$
 (a) Determine the lower cutoff frequency f_L of the filter.
 (b) Draw the frequency response plot of the above filter. [8+8]
5. With the help of logic circuits explain a Multiplexer and a Demultiplexer also give their circuit symbols and give their applications? [16]
6. Explain the basic principles used in PLL. What does the feed back system consist. Explain. [16]
7. (a) What are the advantages of R-2R adder type D/A converter over weighted resistor type?
 (b) In an inverted R-2R ladder, $R=R_f = 22k\Omega$ and $V_R=12V$. Calculate the total current delivered to the op-amp and the output voltage when the binary input 1110. [8+8]
8. Compare the various Logic Families. [16]
