R07

III B.Tech I Semester Examinations, May 2011 SWITCHING THEORY AND LOGIC DESIGN **Mechatronics**

Time: 3 hours

Code No: 07A51403

Max Marks: 80

Answer any FIVE Questions All Questions carry equal marks ****

- 1. Obtain the ASM chart for the following state transition.
 - (a) If x=0 control goes from T_1 to T_2 . If x=1 generate the conditional operation and go from T_1 to T_2 .
 - (b) If x=1 control goes from T_1 to T_2 and then to T_3 . If x=0 control goes from T_1 to T_3 .
 - (c) Start from state T_1 , then if xy=00 go to T_2 , if xy=01, then go to T_3 , if xy=10 then go to T_1 , other wise go to T_3 . Design the control unit using multiplier, decoder and D-flip flops. [16]
- 2. (a) compare combinational versus sequential logic circuits.
 - (b) An equation expressing the next state $Q_n + 1$ in terms of present state Q_n and excitation of the flip flop is called a Characteristic equation. For JK flip flop it is given as $Q_n + 1 = J Q_n^{-1} + K^1 Q_n$. Find the Characteristic equation for T flip flop and D flip flop [8+8]

3. (a) Simplify using K-map
$$F(A, B, C, D, E) = \sum (0, 4, 8, 12, 16, 20, 24, 28)$$

- (b) Simplify using Tabular method $F = \sum (4, 5, 6, 12, 13) + \sum \phi (2, 9, 15)$ [8+8]
- (a) Obtain the 15 bit Hamming code word for the given 11 bit data word:-4. 11001001010.
 - (b) Write out the following decimal weighted codes
 - i. 6,3,1,1 ii. 6,3,1,-1 [8+8]
- (a) Draw the Merger graph and compatibly graph for the given mahine. 5. [8+8]

PS	NS, Z				
	11	12	13	14	
А	-,-	-,-	E,1	-,-	
В	С,0	A,1	В,0	-,-	
С	С,0	D,1	-,-	A,0	
D	-,-	E,1	В,-	-,-	
Е	B,0	-,-	С,-	В,0	

R07

Set No. 2

(b) Construct the Merger table for the given machine.

PS	NX, Z		
	11	12	
Α	Е,0	В,0	
В,	F,0	A,0	
С,	Е,-	С,0	
D	F,-	D,0	
E	С,1	С,0	
F	D,1	B,0	

Code No: 07A51403

- (a) Given the timing diagram (shown below in the fig 1), find the displayed function expressed as a sum of products. Simplify the expression, and also find its inverse.
 - (b) Prove that





- 7. (a) let 'F' be a function for which the product of all true prime implicants is 0. prove that F can not be linearly separable.
 - (b) Prove the functional completeness (Universality) of a threshold gate by realizing AND and OR operations each using a single threshold gate. [8+8]
- 8. (a) Find all the static Hazards in the following circuit figure 2. State the condition under which each hazard can occur. Redesign the circuit so that it is free of static hazards. Use gates with atmost 3 inputs.
 - (b) Design a combinational circuit that converts a 4 bit gray code to a 4 bit binary number. [8+8]



Figure 2



R07

III B.Tech I Semester Examinations, May 2011 SWITCHING THEORY AND LOGIC DESIGN Mechatronics

Time: 3 hours

Code No: 07A51403

Max Marks: 80

Answer any FIVE Questions All Questions carry equal marks

1. Find the equivalence partition and a corresponding reduced machine in a standard form for the given machine. [16]

	NS, Z			
PS	X = 0	$\mathbf{X} = 1$		
А	B,0	E,0		
В	E,0	D ,0		
С	D,1	A,0		
D	C,1	Ε,0		
E	В,0	D,0		
F	C,1	С,1		
G	C,1	D,1		
Н	С,0	A,1		

- 2. (a) Draw the circuit of master-slave RS Flip-Flop and explain its operation with the help of truth table.
 - (b) Convert the following
 - i. JK Flip-Flop to T Flip-Flop.
 - ii. RS Flip-Flop to D Flip-Flop. [8+8]
- 3. (a) Design a 3 bit parity generator using odd parity bit.
 - (b) Design a 2 to 4 decoder using NOR gates only. [8+8]
- 4. For the state diagram shown below in figure 3 draw the ASM chart and design the control unit using D flip flops and a Decoder. [16]



Figure 3:

5. (a) Implement the following function using only NAND gates having a miximum fan in of three

 $f = AB + \bar{A}D + BD + \bar{C}D + AC$

(b) Minimize the following function:

$$f = \sum (0, 1, 2, 3, 4, 6, 10, 11, 12, 13, 14, 15, 16, 29, 31)$$
[8+8]

- 6. (a) Show that the dual of the exclusive OR is equal to its complement
 - (b) Simplify the following

i.
$$F = \overline{\overline{A + B} + C.\overline{D}.E}$$

ii. $F = \overline{\overline{A.B.A.(\overline{A.B}).B}}$
[8+8]

- 7. A ROM chip of 4096×8 bits has two enable inputs and operates from 5V power supply. How many pins are needed for the integrated circuit package. Draw a block diagram and label all input and output terminals in the ROM. [16]
- 8. (a) Determine the possible bases of the number in each operation
 - i. $(41)_3 = 13$
 - ii. 1234+5432=6666
 - (b) in the following series, the same integer is expressed in differen Numer system. Determine the missing mumber of the series 10000, 121,100,?,24,22,20,....
 - (c) Encode each of the 10 decimal digits by means of 8, 7, -4, -2 code [6+5+5]

R07

III B.Tech I Semester Examinations, May 2011 SWITCHING THEORY AND LOGIC DESIGN **Mechatronics**

Time: 3 hours

Code No: 07A51403

Max Marks: 80

[6+10]

Answer any FIVE Questions All Questions carry equal marks ****

- 1. (a) Derive a PLA programming table for the Combinational circuit that squares a 2-bit number.
 - (b) Obtain the PLA programming table for the following two Boolean functions.
 - i. $F_1(x,y,z) = \sum (0,1,2,4)$ ii. $F_2(x,y,z) = \sum (0,5,6,7)$
- 2. (a) What is a race around condition. How is it over come in JK master slave flip flop.
 - (b) Draw the circuit of a clocked SR flip flop using only NAND gates and explain its operation with the help of truth table. |8+8|
- (a) Design a two level code converter code converter from BCD to the 2 -out of 3. -5 code.
 - (b) Find all the static hazards in the following circuit figure 4. State the condition under which each hazard can occur. Redesign the circuit so that it is free of static hazards [8+8]



Figure 4:

- 4. (a) Find the inverse of the following expression $f(A, B, C, D, E) = \left[AB + C(\bar{A} + DE)\right] \left[\bar{B} + A(\bar{E} + \bar{B}\bar{D})\right]$
 - (b) Realize EX-OR of 2 input using 4 number of 2 input NAND gates and EX-NOR of 2 input using 4 number of 2 input NOR gates. [8+8]
- (a) Evaluate a 7 bit composite code word for the data word 0010. Assume an error 5. occurs in bit 5 during writing in into memory. How does this error bit detected and corrected? Explain the procedure to generate the Hamming code.

Code No: 07A51403

R07

Set No. 1

- (b) convert the following numbers from one form to another
 - i. $1000_{10} = (\)_2 = (\)_8$ ii. $110110111_2 = (\)_8 = (\)_{16}$ iii. $7777_8 = (\)_{10} = (\)_2$ [8+8]
- 6. Develop an ASM chart for performing Division using Restoring technique. [16]
- 7. (a) Use the Quire Mc clusky method to determine prime implicants and obtain the minimal expression for the following function.

 $f(v, w, x, y, z) = \sum (13, 15, 17, 18, 19, 20, 21, 23, 25, 27, 29, 31) + \sum \phi(1, 2, 12, 24)$

(b) Simplify the following boolean expression using 4 variable map

 $f(w, x, y, z) = \bar{w}z + xz + \bar{x}y + w\bar{x}z$

- [8+8]
- 8. (a) Find the maximum compatibles for the machines given below.
 - (b) Show the compatibles (BD) and (CD) can be 'deleted'. Find the set of symbolic compatibles and a minimal closed cover for the machine. [16]

PS	NS, Z				
	11	12	13	14	
А	-,-	В,-	-,-	-,1	
В	А,-	-,-	C,0	-,	
С	-,-	-,-	-,-	D,1	
D	В,-	А,-	В,-	F ,0	
Е	С,-	С,-	А,-	-,0	
F	-,0	В,-	-,-	H1	
G	-,1	F,1	E,1	D1	
Η	-,1	G,-	-,-	Е,-	

R07

III B.Tech I Semester Examinations, May 2011 SWITCHING THEORY AND LOGIC DESIGN **Mechatronics**

Time: 3 hours

Code No: 07A51403

Max Marks: 80

Answer any FIVE Questions All Questions carry equal marks ****

- 1. (a) Design a code converter circuit which converts decimal code to excess-3 code realize the circut.
 - (b) Find POS and SOP for the given function using K-map $f = ABD + ACD + C\bar{D} + AD + D$
- 2. (a) While every maximal compatible prime compatible, every machine may not be a symbolic compatible. Justify this statement. In the given below, show at least one machine which in not a symbolic compatible.
 - (b) Reduce the machine given below.

[8+8]

[16]

[8+8]



- (a) Implement a 4 to 1 digital MUX using a decode and 4 tristate buffers. 3.
 - (b) What is the difference between encode and digital multiplexes?
 - (c) Give 4 applications of a decode. [16]
- 4. Design a BCD counter using T-flip flops.
- 5. (a) Decode the following 12bit Hamming code words and obtain the original 8bit data word
 - i. 000011101010
 - ii. 101111110100
 - (b) Perform the following decimal addition for use with
 - i. 8421 BCD code and
 - [8+8]ii. Excess-3Code $(123)_{10} + (987)_{10}$
- 6. (a) Given 32×8 ROM chip with Enable input, show the external connections necessary to construct a 128×8 ROM with four chips and a decoder.
 - (b) Explain the Linear Separability property of a Threshold function. [8+8]

www.firstranker.com

R07

Set No. 3

[8+8]

- 7. Design a control for the state table given using two multiplexers, a register and a decoder. [16]
- 8. (a) Prove the following:

Code No: 07A51403

- i. $A \oplus B = \overline{A} \oplus \overline{B}$ ii. $A \oplus (B + C) = (A \oplus B) + (A \oplus C)$ iii. If $A \oplus B \oplus C = D$, then $A \oplus B = C \oplus D$ and $A = B \oplus C \oplus D$.
- (b) Find the dual of the following expressions:
 - i. $x + (\overline{x}\overline{y} + \overline{x}\overline{z})$
 - ii. Vwx + Vwyz + wxy + Vxyz.