Code No: 07A5EC01 **R07** **Set No. 2**

III B.Tech I Semester Examinations,MAY 2011
COMPUTER SYSTEM ORGANIZATION
Electrical And Electronics Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Explain the following:
   (a) Magnetic Tape Systems
   (b) Optical Disc
   (c) DVD Technology. [16]
2. (a) What are the different physical forms available to establish an inter- connection network? Give the summary of those.
   (b) Explain time-shared common bus Organization.
   (c) Explain system bus structure for multiprocessors. [16]
3. (a) What is polling? Explain in detail.
   (b) What is daisy chaining priority? Explain. [8+8]
4. Explain the following with related to the Instruction Pipeline.
   (a) Pipeline conflicts
   (b) Data dependency
   (c) Hardware interlocks
   (d) Operand forwarding
   (e) Delayed load
   (f) Pre-fetch target instruction
   (g) Branch target buffer
   (h) Delayed branch. [16]
5. An instruction is stored at location 300 with its address field at location 301 with a value 400. A processor register R1 contains the number 200. Calculate the effective address if the addressing mode of the instruction is Direct, Indirect, Relative, Register Indirect and index (with the process register as an index register). [16]
6. (a) Give the short sequence of machine instructions for the task "Add the contents of memory location A to those of location B and place the answer in location C". Using Add, Load and Store instructions.
   (b) Convert the decimal numbers to the bases indicate.
      i. 7562 to octal

ii. 1938 to hexadecimal [16]

7. Write in detail about the design of hard wired control unit. [16]

8. A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts, an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part.

   (a) How many bits are there in the operation code, a register code part, and the address part?

   (b) Draw the instruction word format and indicate the number of bits in each part.

   (c) How many bits are there in the data and address inputs of memory? [16]

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Code No: 07A5EC01 **R07** **Set No. 4**

III B.Tech I Semester Examinations,MAY 2011
COMPUTER SYSTEM ORGANIZATION
Electrical And Electronics Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Draw the diagram for connection between the processor and the memory and explain basic operational concepts of computer.
   (b) Write about bus structures. [8+8]
2. Explain Data transfer and Program control instructions. [16]
3. (a) What is polling? Explain in detail how it can be used for interprocessor arbitration.
   (b) Explain the organization of tightly coupled multiprocessor system with a generic block diagram. [8+8]
4. (a) Write about various types of ROMs.
   (b) Explain virtual-memory address translation. [8+8]
5. How many characters per second can be transmitted over a 1200-band line in each of the following modes with a character code of 8 bits?
   (a) Synchronous serial transmission.
   (b) Asynchronous serial transmission with two stop bits
   (c) Asynchronous serial transmission with one stop bits [16]
6. (a) Explain in detail various fields of microinstruction format with diagram.
   (b) Describe how microinstructions are arranged in control memory and how they are interpreted. [8+8]
7. (a) Is it reasonable to classify a Branch Target Buffer (BTB) as just one more cache in a machine? Why?
   (b) A 32-bit machine has a 512 entry branch target buffer. Draw a diagram of this BTB. Assuming direct mapping, how many bits of storage does this BTB require? [8+8]
8. The content of AC in the basic computer is hexadecimal A937 and the initial value of E is 1. Determine the contents of AC, E , PC, AR , and IR in hexadecimal after the execution of the CLA instruction. Repeat 11 more times, starting from each one of the register-reference instructions. The initial value of PC is hexadecimal 021. [16]

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Code No: 07A5EC01 **R07** **Set No. 1**

III B.Tech I Semester Examinations,MAY 2011
COMPUTER SYSTEM ORGANIZATION
Electrical And Electronics Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain address sequencing in Microprogrammed control unit
   (b) Explain in detail various fields of microinstruction format with diagram. [8+8]
2. (a) Explain the following:
      i. Optical Disc
      ii. DVD Technology.
   (b) Describe the two update policies that a cache can use. For each policy, give an example of a situation where it would be preferred. [8+8]
3. (a) What is pipelining? Explain.
   (b) Explain four segment pipelining. [8+8]
4. (a) Define the following terms and their usage.
   PC,MAR,MDR,ALU,IR,R0,R1.
   (b) "Having a large number of processor registers makes it possible to reduce the number of memory accesses needed to perform complex tasks". Devise a simple computational task to show the validity of this statement for a processor that has four registers compared to another that has only two registers.[8+8]
5. (a) When is the interrupt service routine for a device invoked? Upon the occurrence of an interrupt, how does the processor determine the memory address of the correct service routine. What is the status of interrupted program during and after interrupt.
   (b) Which is the most efficient in the following?
      i. Programmed I/O
      ii. Interrupt Initiated I/O
      iii. DMA
      Justify your answer [8+8]
6. (a) What is cache coherence? Explain.
   (b) What are the conditions for incoherence?
   (c) Explain the solutions to the cache coherence problem. [5+5+6]
7. Draw the flow chart for memory reference instruction execution with control functions and RTL statements. [16]
8. (a) Explain the operation of control unit of basic computer with diagram.

(b) Suppose a 32-bit instruction takes the following format:
[OPCODE DR SR1 SR0 UNUSED]
If there are 225 opcodes, 120 registers:

i. What is the minimum number of bits required to represent the OPCODE?
ii. What is the minimum number of bits required to represent the Destination Register (DR)?
iii. What is the maximum number of UNUSED bits in the instruction encoding?
iv. What is the maximum number of offset bits? [8+8]

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Code No: 07A5EC01 **R07** **Set No. 3**

III B.Tech I Semester Examinations,MAY 2011
COMPUTER SYSTEM ORGANIZATION
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) What are the different interconnection structures used in multiprocessors?
   (b) Explain the functioning of Binary Tree network with 2 x 2 switches. Show with a neat sketch. [8+8]
2. (a) Explain about strobe signal and handshaking in detail.
   (b) What are the different kinds of DMA transfers? What are the advantages of using DMA transfers? [8+8]
3. (a) What are computer registers. And give their functionality.
   (b) Sketch the register transfers for the fetch phase.
   (c) What are the phases of an instruction cycle? [16]
4. (a) List the 10 BCD digits with an even parity in the left most position (total five digits per bit) Repeat with an odd parity bit.
   (b) Perform the arithmetic operations (+42) + (-13) and (-42) - (-13) in binary using signed 2'compliment representation for negative numbers. [8+8]
5. (a) Differentiate between microprogramming and nanoprogramming.
   (b) "Hardwired control unit is faster than microprogammed control unit". Justify this statement. [8+8]
6. Discuss the following with examples.
   (a) Zero-address instructions
   (b) One-address instructions
   (c) Two-address instructions
   (d) Three-address instructions [16]
7. (a) A block set-associative cache consists of a total of 64 blocks divided into 4-block sets. The main memory contains 4096 blocks, each consisting of 128 words.
      i. How many bits are there in a main memory address?
      ii. How many bits are there in each of the TAG, SET, and WORD fields?
   (b) Explain the organization of a 1K x 1 memory with a neat sketch. [8+8]
8. (a) Formulate six-segment pipeline for a computer. Specify the operations to be performed in each segment.

(b) Give an example of a program that will cause data conflict in the three-segment pipeline. [8+8]

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