Code No: 07A5EC07 **R07** **Set No. 2**

III B.Tech I Semester Examinations,May 2011
COMPUTER ORGANIZATION
Common to Electronics And Telematics, Electronics And Instrumentation Engineering, Electronics And Communication Engineering
Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain the key design elements of most RISC systems.
   (b) Differentiate between RISC and CISC. [8+8]
2. (a) Explain data dependency?
   (b) Explain handling of branch instructions?
   (c) Explain vector operations? [6+6+4]
3. (a) Explain the advantage of subroutine register in a control unit.
   (b) How do you map micro operation to a micro instruction address? [8+8]
4. (a) Explain about the normalization and biased exponent.
   (b) Explain about positive overflow and negative overflow condition of floating point numbers. [8+8]
5. (a) List and discuss about the function of system software.
   (b) Explain how user program and OS routines are sharing the processor. [8+8]
6. (a) Explain about page replacement in virtual memory?
   (b) Differentiate address space and memory space?
   (c) Draw the diagram showing memory connections to the CPU in which memory capacity is 512 bytes of RAM and 512 bytes of ROM. [6+4+6]
7. (a) Obtain the truth table of an 8*3 priority encoder. Assume that the three outputs xyz from the priority encoder are used to provide a vector address of the form 101xyz00. List the 8 vector addresses starting from the one with the highest priority.
   (b) What programming steps are required to check when a source interrupt the computer while it is still being serviced by a previous interrupt request from the same source. [8+8]
8. (a) What is cache coherence, and why is it important in shared memory multiprocessor systems? How can the problem be resolved with a snoopy cache controller?

(b) Consider a bus topology In which two processors communicate through a buffer in shared memory. When one processor wishes to communicate with other processor it puts the information in the memory buffer and sets a flag. Periodically, the other processor checks the flags to determine if it has information to receive. What can be done to ensure proper synchronization and to minimize the time between sending and receiving the information. [8+8]

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Code No: 07A5EC07 **R07** **Set No. 4**

III B.Tech I Semester Examinations,May 2011
COMPUTER ORGANIZATION
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain Time-Shared common bus?
   (b) Explain multiport memory with diagram? [8+8]
2. (a) Explain micro instruction format with a neat diagram.
   (b) List the symbols for various micro instruction fields. [8+8]
3. (a) Explain the terms : Compilers, Linkers, Loaders, Assemblers.
   (b) Describe the program execution in a system with a neat diagram. [8+8]
4. (a) Explain Read and Write operations in an associative memory?
   (b) Explain about direct mapping of cache memory?
   (c) Explain Read and Write operations in cache memory? [5+6+5]
5. Explain Priority Interrupt in detail? [16]
6. Explain Instruction Pipe line in detail? [16]
7. Design the circuit which can be used to transfer data from any register to any other register out of four 4-bit registers A, B, C, D which uses RS flip flops. [16]
8. Derive an algorithm in flowchart form for adding and subtracting two fixed point binary numbers when negative numbers are in signed 1'S complement representation. [16]

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Code No: 07A5EC07 **R07** **Set No. 1**

III B.Tech I Semester Examinations,May 2011
COMPUTER ORGANIZATION
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Explain cache memory in detail with all the mapping procedures? [16]
2. (a) Write the characteristics of multi processors?
   (b) Explain interprocessor arbitration in detail? [8+8]
3. (a) State the basic reason why 2'S complement representation of signed integers are used in computer systems.
   (b) Represent the decimal number -0.75 in single and double precision formats. [8+8]
4. (a) Explain about the branch field of micro operation.
   (b) Discuss the symbolic microinstructions fields? [8+8]
5. (a) Explain about expanded structure of IAS computer with neat diagram. [16]
6. Give an account of:
   (a) Program control instructions
   (b) Conditional branch instructions [2X8=16]
7. (a) Consider the multiplication of two 20*20 matrices using a vector processor.
      i. How many product terms are there in each inner product, and how many inner products must be evaluated?
      ii. How many multiply-add operations are needed to calculate the product matrix?
   (b) Determine the number of clock cycles that it takes to process 100 tasks in a 3-segment pipe line. [8+8]
8. (a) Explain Asynchronous Data Transfer.
   (b) Design a parallel priority interrupt hardware for a system with 8 interrupt sources. [8+8]

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Code No: 07A5EC07 **R07** **Set No. 3**

III B.Tech I Semester Examinations,May 2011
COMPUTER ORGANIZATION
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Define addressing mode. What is the purpose of addressing modes and explain different types of addressing modes. [16]

2. (a) Draw the diagram for 4-segment CPU pipeline.
   (b) What is Delayed branch ? Explain? [8+8]

3. (a) Explain how to evaluate the performance of a computer.
   (b) Why 2's compliment representation of data is preferable in fixed point representation. [10+6]

4. (a) Draw and explain the hardware for signed magnitude addition and subtraction.
   (b) Draw and explain the hardware for signed 2'S complement addition and subtraction.
   [8+8]

5. (a) A virtual memory has a page size of 1K words. There are 8 pages and 4 blocks. The associative memory page table contains the following entries:

Page	Block
0	3
1	1
4	2
6	0

   Make a list of all virtual addresses in decimal that will cause a page fault if used by the CPU.
   (b) A magnetic disk system has the following parameters:
   Tx = average time to position the magnetic head over a track
   R = rotation speed of disk in revolutions per second
   Nt = number of bits per track
   Ns = number of bits per sector
   Calculate the average time Ta that it will take to read one sector [10+6]

6. (a) Draw the hypercube structures for n = 1,2,3
   (b) Draw the diagram for parallel arbitration logic and explain? [8+8]

7. (a) Explain in brief why hardwired control unit does not sufficient to generate control signals for complex machine instructions.

(b) What is the function of the control address register in a micro programmed control unit. [8+8]

8. (a) How many characters per second can be transmitted over a 1200-baud line in each of the following modes? Assume a character code of 8-bits
   i. Synchronous serial transmission
   ii. Asynchronous serial transmission with two stop bits
   iii. Asynchronous serial transmission with one stop bit

   (b) Explain Isolated versus Memory-Mapped I/O [8+8]

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