Code No: 07A60403 **R07** **Set No. 2**

III B.Tech II Semester Examinations,APRIL 2011
LINEAR AND DIGITAL I.C. APPLICATIONS
Mechatronics

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Design a conversion circuit to convert a JK flip-flop to T flip-flop?
   (b) Write short notes on serial in serial out shift register. [8+8]
2. (a) Draw the circuit of a Weighted Resistor DAC and obtain expression for n-bits.
   (b) Sketch the Analog output voltage for the given digital input code. Assume any data.
   (c) What are the major disadvantages in a weighted resistor DAC? [8+4+4]
3. (a) Classify the filters and explain the characteristics of each one of them.
   (b) Draw the first order low-pass Butterworth filter and analyze the same by deriving the gain and phase angle equation. [8+8]
4. List out standard TTL Characteristics and explain them briefly with necessary diagrams. [16]
5. (a) With the help of logic diagram explain 74×157 multiplexer?
   (b) Design a serial binary adder? [8+8]
6. (a) Explain the application of three terminal adjustable voltage regulator.
   (b) With the help of block diagram explain LF398 sample and hold IC along with wave forms. [8+8]
7. (a) For an inverting Op-amp having $R_1 = 470\Omega$, feedback resistor $R_F = 4.7K\Omega$ and Calculate Closed loop gain, Bandwidth with feed back, Input resistance, Output Resistance.
   (b) Derive the formulae used in solving part (a). [8+8]
8. (a) Give the functional block diagram of NE 565 PLL and for the given component values. $C_1 = 390$PF, $C_2 = 680$PF and $R_1 = 10$k,$V_{cc} = \pm 6$V. Find
      i. The free running frequency.
      ii. The lock range and capture range.

      Where C_1 is the capacitor connected between pin number 9 and - V_{CC}, C_2 is the capacitor connected between + V_{CC} and output pin 7, and R_1 is connected between pin number 8 and + V_{CC}.
   (b) Give the functional block diagram of VCO NE566 and explain its working and necessary expression for free running or center frequency. [16]

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Code No: 07A60403 **R07** **Set No. 4**

III B.Tech II Semester Examinations,APRIL 2011
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Mechatronics

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Write a short notes on synchronous down counter.
   (b) Give the applications, advantages and disadvantages of ROM. [8+8]
2. (a) What is a decoder? Write short notes on Binary decoder?
   (b) Write short notes on Excess 3 to BCD code converter. [8+8]
3. (a) Illustrate one application each of Analog to Digital and Digital to Analog converters.
   (b) Describe in detail the operation of a dual slope Analog to digital converter.
   (c) List out and compare different types of A/D converters. [4+7+5]
4. (a) Explain how the input off set voltage compensated for Op-amp. [6+6+4]
   (b) How fast can the output of an Op-amp change by 10V, if its slew rate is 1V/μs?
   (c) Define thermal drift.
5. (a) Sketch the circuit of a logarithmic amplifier using one Op-amp and explain its operation. State its application.
   (b) What is a sample and hold circuit? Why is it needed? Draw a sample and hold circuit and explain its operation. [8+8]
6. (a) Calculate the frequency of oscillation of a 566 VCO IC for the external component values $R_T = 6.8K\Omega$ and $C_T = 470PF$. Assume other component values if necessary. Shown in figure 6b.
   (b) Derive the expression for frequency of VCO and list important specifications of 566 VCO IC. [8+8]

Code No: 07A60403 **R07** **Set No. 4**

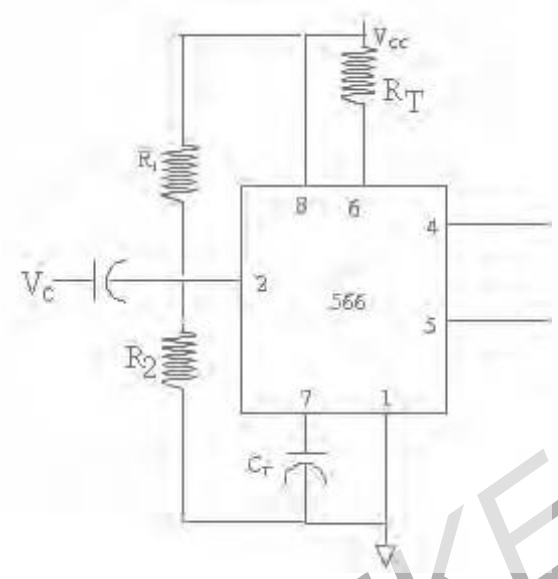

Figure 6b

7. (a) Discuss interfacing of logic families with examples.
   (b) Explain sinking current and sourcing current of TTL output? Which of the above parameters decide the fan out and how? [8+8]

8. (a) With necessary external components to a VCO IC NE556, Explain the generation of a triangular wave.
   (b) A PLL has a free running frequency of 500 KHz, the bandwidth of the LPF=10 KHz. Will the PLL lock in if f_i =60 KHz? What is the frequency of the VCO outputs? [10+6]

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Code No: 07A60403 **R07** **Set No. 1**

III B.Tech II Semester Examinations,APRIL 2011
LINEAR AND DIGITAL I.C. APPLICATIONS
Mechatronics

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Draw the circuit of a Ladder type DAC for 4 bits and derive expression for output voltage.
   (b) Sketch the Analog output voltage for the given digital code. Assume any data.
   (c) Compare R-2R and Weight Resistor types of ADC. [8+4+4]
2. (a) For a second order low pass Butterworth filter show that $f_H = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}}$
   (b) Design a wide band-pass filter with f_L=400 Hz,f_H=2 KHz and pass band gain=4. Also draw an approximate frequency response plot of the filter shown in figure 2b. [8+8]

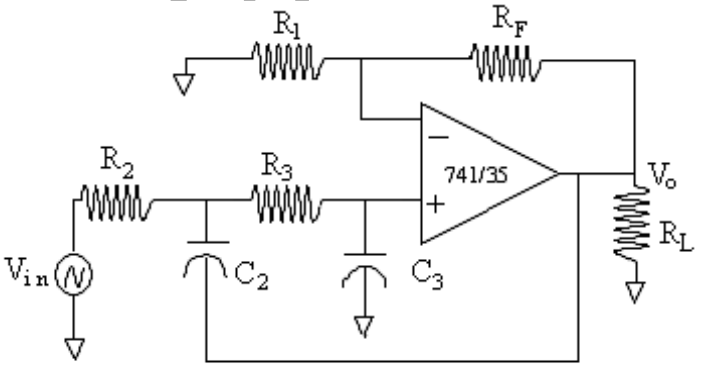

Figure 2b

3. (a) Explain the significance of each of comparator in 555 timer and also explain its operation.
   (b) Explain the application of 555 timer as Linear ramp generator. [8+8]
4. (a) Write short notes on synchronous up counter.
   (b) Explain the operation of Synchronous SRAM with the help of its internal Architecture. [8+8]
5. (a) Discuss the operation of a log amplifier and derive the expression for output voltage.
   (b) Design a current to voltage converter using Op-amp and explain how it can be used to measure the output of a photocell. [8+8]
6. (a) Draw the pin diagram and schematic symbol of a typical Op-amp IC741 and explain the function of each pin. [6+6+4]

(b) Discuss the three basic types of linear IC packages and briefly explain the characteristics of each.

(c) State the two types of integrated circuits classified according to their mode of operation and briefly explain the significance of each.

7. (a) Explain how to estimate sinking current for low output and sourcing current for high output of CMOS gate?

(b) Analyze the fall time of CMOS inverter output with $R_L = 1K\Omega$ $V_L = 2.5V$ and $C_L = 100PF$. Assume V_L as stable state voltage. [8+8]

8. (a) Design the 32 input to 5 output priority encoder using four 74LS148 and gates?

(b) Design a CMOS transistor circuit with the functional behavior $F(X) = (A + \overline{B})(B + \overline{D})(A + \overline{D})$. [8+8]

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Code No: 07A60403 **R07** **Set No. 3**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) Write short notes on serial in parallel out shift register.
   (b) Design a conversion circuit to convert a D flip-flop to T flip-flop? [8+8]
2. (a) Write short notes on non inverting comparator.
   (b) For the given (figure 2b) inverting Schmitt trigger, calculate its higher and lower trigger levels. [8+8]

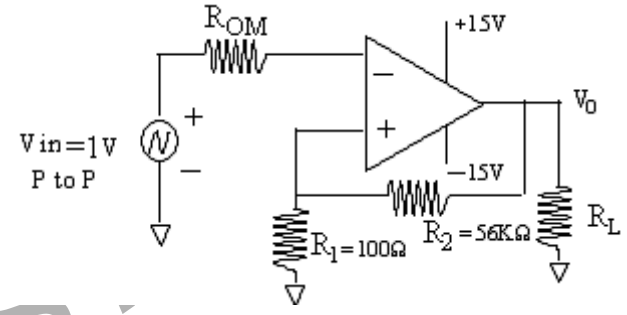

Figure 2b

3. Explain the functional block diagram of PLL emphasizing the importance of capture range and Lock range. [16]
4. (a) Design a 3 input 5-bit multiplexer? Write the truth table and draw the logic diagram.
   (b) Write short notes on full subtractor. [8+8]
5. (a) A fourth order Butterworth polynomial is given as (S^2+0.765S+1) (S^2 + 1.848S+1). Design the fourth order Butterworth filter having upper cutoff frequency 2 KHz. Assume suitable data. Draw the circuit diagram with suitable values.
   (b) What are the gain constraints imposed on higher order filters? Explain.[10+6]
6. (a) Design a 4-bit binary weighted DAC, also find out the step size of the output for all combinations of input and plot its transfer characteristics curve.
   (b) Give the schematic circuit diagram of the fastest A/D converter and explain its operation. [8+8]
7. (a) Define the following electrical parameters of an Op-amp:
      i. input offset current
      ii. input bias current,

iii. Differential input resistance
iv. input capacitance
v. offset voltage adjustment range and
vi. CMRR.

(b) Determine the output voltage in each of the following cases for the open loop differential amplifier shown in figure 7b.

i. $V_{in1} = 5\mu V$ dc $V_{in2} = -7\mu V$ dc
ii. $V_{in1} = 10mV$ (rms) Vin2 = 20 mV (rms)
The Op-amp has the following specifications = 200000, $R_i = 2M\Omega$, $R_o = 75\Omega$, $V_{cc} = +15V$, $V_{EE} = -15V$ and output swing = $\pm 14V$.[10+6]

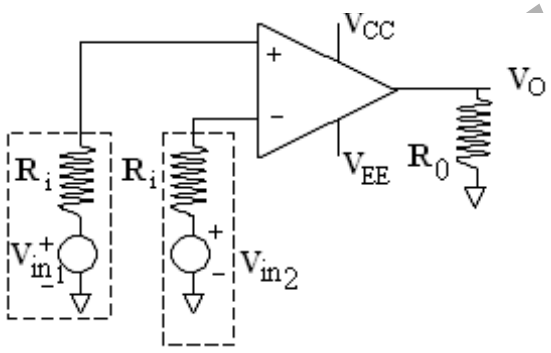

Figure 7b

8. (a) Draw the logic diagram equivalent to the internal structure of an 8-input CMOS NAND gate? Show the transistor circuit for this gate and explain the operation with the help of function table?

(b) Draw the circuit diagram of basic CMOS gate and explain the operation? [12+4]

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