

CODE NO: 07A6EC01

R07

SET No - 1

**III B.TECH - II SEMESTER EXAMINATIONS, APRIL/MAY, 2011**  
**DIGITAL SIGNAL PROCESSING**  
**(COMMON TO EEE, ECE, EIE, ETM, ICE)**

Time: 3hours

Max. Marks: 80

**Answer any FIVE questions**  
**All Questions Carry Equal Marks**

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- 1.a) Define an LTI System and show that the output of an LTI system is given by the convolution of Input sequence and impulse response.
- b) Prove that the system defined by the following difference equation is an LTI system  $y(n) = x(n+1) - 3x(n) + x(n-1)$ ;  $n \geq 0$ . [8+8]
- 2.a) Define DFT and IDFT. State any Four properties of DFT.
- b) Find 8-Point DFT of the given time domain sequence  $x(n) = \{1, 2, 3, 4\}$ . [8+8]
- 3.a) Derive the expressions for computing the FFT using DIT algorithm and hence draw the standard butterfly structure.
- b) Compare the computational complexity of FFT and DFT. [8+8]
4. Discuss and draw various IIR realization structures like Direct form – I, Direct form-II, Parallel and cascade forms for the difference equation given by  $y(n) = -3/8 Y(n-1) + 3/32 y(n-2) + 1/64 y(n-3) + x(n) + 3 x(n-1) + 2 x(n-2)$ . [16]
- 5.a) Compare Butterworth and Chebyshev approximation techniques.
- b) Design a Digital Butterworth LPF using Bilinear transformation technique for the following specifications  
 $0.707 \leq |H(w)| \leq 1$ ;  $0 \leq w \leq 0.2\pi$   
 $|H(w)| \leq 0.08$ ;  $0.4 \pi \leq w \leq \pi$  [8+8]
- 6.a) Compare FIR and IIR filters
- b) Design an FIR Digital High pass filter using Hamming window whose cut off freq is 1.2 rad/s and length of window  $N=9$ . [8+8]
- 7.a) Define Multirate systems and Sampling rate conversion
- b) Discuss the process of n Decimation by a factor D and explain how the aliasing effect can be eliminated. [8+8]
8. Discuss various Modified Bus structures of Programmable DSP Processors.[16]

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- 1.a) Write short notes on classification of systems.
- b) Derive BIBO stability criteria to achieve stability of a system. [8+8]
- 2.a) Define DFS. State any Four properties of DFS.
- b) Find the IDFT of the given sequence  $x(K) = \{2, 2-3j, 2+3j, -2\}$ . [8+8]
- 3.a) Find  $X(K)$  of the given sequence  $x(n) = \{1, 2, 3, 4, 4, 3, 2, 1\}$  using DIT-FFT algorithm.
- b) Compare the computational complexity of FFT and DFT. [8+8]
4. What are the various basic building blocks in realization of Digital Systems and hence discuss transposed form realization structures.
- 5.a) Compare Impulse Invariant and Bilinear transformation techniques.
- b) Compute the poles of an Analog Chebyshev filter TF that satisfies the Constraints  
 $0.707 \leq |H(j\Omega)| \leq 1 ; 0 \leq \Omega \leq 2$   
 $|H(j\Omega)| \leq 0.1 ; \Omega \geq 4$   
and determine  $H_a(s)$  and hence obtain  $H(z)$  using Bilinear transformation. [16]
- 6.a) Derive the conditions to achieve Linear Phase characteristics of FIR filters
- b) Design an FIR Digital Low pass filter using Hanning window whose cut off freq is 2 rad/s and length of window  $N=9$ . [8+8]
- 7.a) Discuss the implementation of Polyphase filters for Interpolators with an example
- b) Discuss the sampling rate conversion by a factor  $I/D$  with the help of a Neat block Diagram. [8+8]
8. Write short notes on:
  - a) VLIW Architecture of Programmable Digital Signal Processors
  - b) Multiplier and Multiplier Accumulator [8+8]

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**Time: 3hours****Max. Marks: 80**

**Answer any FIVE questions**  
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- 1.a) Discuss various discrete time sequences.
- b) Give the Basic block diagram of Digital Signal Processor. [8+8]
- 2.a) Define DFS. State any Four properties of DFS.
- b) Find the IDFT of the given sequence  $x(K) = \{2, 2-3j, 2+3j, -2\}$ . [8+8]
- 3.a) Find IFFT of the given  $X(K) = \{1, 2, 3, 4, 4, 3, 2, 1\}$  using DIF algorithm
- b) Bring out the relationship between DFT and Z-transform. [8+8]
- 4.a) Define Z-Transform and List out its properties.
- b) Discuss Direct form, Cascade and Linear phase realization structures of FIR filters. [8+8]
- 5.a) Discuss digital and analog frequency transformation techniques.
- b) Discuss IIR filter design using Bilinear transformation and hence discuss frequency warping effect. [8+8]
- 6.a) Compare various windowing functions.
- b) Design an FIR Digital Low pass filter using rectangular window whose cut off freq is 2 rad/s and length of window  $N=9$ . [8+8]
- 7.a) Define Interpolation and Decimation. List out the advantages of Sampling rate conversion.
- b) Discuss the sampling rate conversion by a factor I with the help of a Neat block Diagram. [8+8]
- 8.a) Discuss Various Addressing modes of Programmable Digital Signal Processors.
- b) Give the Internal Architecture of TMS320C5X 16 bit fixed point processor.[8+8]

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**Answer any FIVE questions**  
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- 1.a) Define Linearity, Time Invariant, Stability and Causality.
- b) The discrete time system is represented by the following difference equations in which  $x(n)$  is input and  $y(n)$  is output.  $Y(n) = 3y^2(n-1) - nx(n) + 4x(n-1) - 2x(n-1)$ . [8+8]
- 2.a) Define Convolution. Compare Linear and Circular Convolution techniques.
- b) Find the Linear convolution of the given two sequences  $x(n) = \{1, 2\}$  and  $h(n) = \{1, 2, 3\}$  using DFT and IDFT. [8+8]
- 3.a) Develop DIT-FFT algorithm and draw signal flow graphs for decomposing the DFT for  $N=6$  by considering the factors for  $N = 6 = 2 \cdot 3$ .
- b) Bring out the relationship between DFT and Z-transform. [8+8]
- 4.a) Discuss transposed form structures with an example.
- b) Discuss Direct form, Cascade realization structures of FIR filters. [8+8]
- 5.a) Discuss digital and analog frequency transformation techniques.
- b) Discuss IIR filter design using Impulse Invariant transformation and list out its advantages and Limitations. [8+8]
- 6.a) Compare various windowing functions
- b) Design an FIR Digital Band pass filter using rectangular window whose upper and lower cut off freq.'s are 1 & 2 rad/s and length of window  $N = 9$ . [8+8]
- 7.a) Define Interpolation and Decimation.
- b) Discuss the sampling rate conversion by a factor I/D with the help of a Neat block Diagram. [8+8]
- 8.a) Write a short notes on On-Chip peripherals of Programmable DSP's.
- b) Give the Internal Architecture of TMS320C5X 16 bit fixed point processor. [8+8]

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