

Code No: 07A6EC03

**R07****Set No. 2**

III B.Tech II Semester Examinations, APRIL 2011

VLSI DESIGN

Common to BME, ETM, E.CONT.E, ECE, EEE

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions  
All Questions carry equal marks

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1. (a) Explain the processing steps in fabrication of PMOS technology with neat sketches.  
(b) What are the additional two layers in BICMOS technology compared to other. [10+6]
2. (a) Derive the relation between  $I_{DS}$  &  $V_{DS}$  of MOSFET.  
(b) Draw the circuit for NMOS inverter and explain its operation. [8+8]
3. Explain about Testing and Fault Simulation in VLSI Design. [16]
4. (a) Explain about Technology Libraries used in synthesis tools.  
(b) How delay effects are used in synthesis process. [8+8]
5. (a) Derive the expression for  $\tau_{SD}$  in the case of a MOSFET.  
(b) Explain about sheet resistance and sheet capacitance. [8+8]
6. (a) Explain about bit sliced Data path organization. What is the significance of Data paths in digital processors?  
(b) Give the Truth Table for full adder and explain its Boolean expression. [8+8]
7. (a) Why scaling is required?  
(b) How does Depletion Regions around Source and Drain are affected due to scaling down of device dimensions? Explain. [6+10]
8. (a) With the help of a block diagram explain the principle and operation of standard cells.  
(b) Explain about different levels of abstraction. [10+6]

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1. Explain about oxidation, Diffusion and Ion Implantation Processes of I C Fabrication. [16]
2. Draw the schamactic for PLA and explain the principle. What are the advantages of PLAs? [16]
3. (a) Draw the stick diagram and layout for the following function  
 $f = A \bar{B} + \bar{A}C + B\bar{C}$   
(b) What is the difference between ' $\alpha$ ' and ' $\beta$ ' scaling factors? Give some examples. [8+8]
4. With the help of a schematic explain the principle of Tree Multiplier. [16]
5. With a schematic explain about synthesis process. [16]
6. Draw the circuit for nMOS Inverter and explain its operation and characteristics. [16]
7. (a) Explain about BICMOS Driver circuits.  
(b) Derive the expression for propagation delay  $\tau_D$  in the case of cascaded pass Transistors. [8+8]
8. (a) What are the different categories of DFT techniques? Explain.  
(b) What is meant by signature analysis in Testing? Explain with an example. [8+8]

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1. Explain about Placement and Routing in VLSI Design. [16]
2. (a) Derive the expressions for Rise-Time  $\tau_R$  and fall time  $\tau_f$  in the case of CMOS Inverter.  
(b) Express the Area capacitance interms of standard capacitance units. [10+6]
3. Explain about the principle and operation of FPGAs. What are its applications? [16]
4. What are the circuit design considerations in the case of static adder circuits. [16]
5. (a) Explain about Design Rule Check. Why is it employed?  
(b) For various processes in MOS IC fabrication, explain about Design Rules. [8+8]
6. (a) With the help of a schematic explain about Memory-self Test.  
(b) What are the issues to be considered while implementing BIST? Explain. [8+8]
7. (a) What is the purpose of metallisation in I.C. manufacturing? Explain the methods employed for metallisation.  
(b) What is probe testing? Why it is used? [10+6]
8. For the circuit shown in figure 1 calculate  $I_D$  and  $V_{Ds}$ 
  - (a) if  $K_n = 120\mu A/v^2$ ,  $V_{tn} = 0.6v$  &  $(\frac{w}{L})$  for the MOSFET M is 4.
  - (b) Draw the circuit for CMOS inverter and explain its characteristics. [8+8]

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Set No. 1

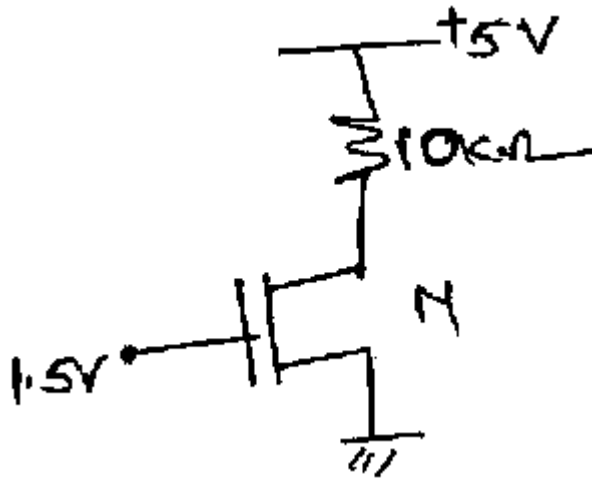


Figure 1

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FIRSTRANKER

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**R07****Set No. 3**

III B.Tech II Semester Examinations, APRIL 2011

VLSI DESIGN

Common to BME, ETM, E.CONT.E, ECE, EEE

Time: 3 hours

Max Marks: 80

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All Questions carry equal marks

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1. Explain about the process steps

- (a) Crystal Growth
- (b) Oxidation
- (c) Diffusion
- (d) Lithography
- (e) Matallisation

involved in the fabrication of ICs. [16]

- 2. (a) Draw the CMOS circuit to realize the Boolean expression  $y=A-B$ , and explain the same.
- (b) What is meant by fan in & fanout of gate. [10+6]
- 3. (a) How layout design can be done for improving testability? Explain.
- (b) Explain about different fault models in VLSI testing with examples. [8+8]
- 4. For nMOS Inverter driven by another nMOS Inverter, derive the expression for  $\frac{Z_{pu}}{Z_{pd}}$  ratio. [16]
- 5. (a) What are the various constraints in Synthesis Process? Explain.

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Set No. 3

- (b) Using block schematics, explain about attributes in synthesis process. [8+8]
6. Give the schematic for a  $4 \times 4$  carry-save multiplier and explain its operation. [16]
7. Compare PLAs, PALs, CPLDs, FPGAs, and standard cells in all respects. [16]
8. Due to scaling and smaller dimensions of MOSFETs, explain the effect on
- (a) Drain Induced Barrier lowering
  - (b) Lower Transconductance
  - (c) Inter - connect capacitance. [6+6+4]

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FIRSTRANKER