Code No: 07A6EC14   **R07**   **Set No. 2**

III B.Tech II Semester Examinations,APRIL 2011
COMPUTER ORGANIZATION
Mechatronics

Time: 3 hours   Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks
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1. (a) Differentiate between RAM and ROM in terms of structure, operation and organization.

   (b) Write about Vectored interrupts.   [8+8]

2. Design parallel priority interrupt hardware for a system with eight interrupt sources.
                                                                          [16]

3. (a) Give an example for four stage instruction pipeline and also explain the operation using flow chart.

   (b) Explain the problems that cause the instruction pipeline to deviate from its normal operation.   [8+8]

4. Write in detail about the design of Micro programmed control unit.   [16]

5. An instruction is stored at location 300 with its address field at location 301 with a value 400. A processor register R1 contains the number 200. Calculate the effective address if the addressing mode of the instruction is Direct, Indirect, Relative, Register Indirect and index (with the process register as an index register).   [16]

6. Differentiate between serial arbitration and parallel arbitration .   [16]

7. (a) Derive an algorithm in flowchart form for adding and subtracting two fixed-point binary numbers when negative numbers are in signed-1,s complement representation.

   (b) Explain multiplication algorithm for signed-magnitude data with examples.
                                                                          [8+8]

8. (a) Derive the circuit for a 3 bit parity generator and 4 bit parity checker using an odd parity bit.

   (b) Having a large number of processor registers makes it possible to reduce the number of memory accesses needed to perform complex tasks? Devise a simple computational task to show the validity of this statement for a processor that has four registers compared to another that has only two register.   [8+8]

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Code No: **07A6EC14** | **R07** | **Set No. 4**

III B.Tech II Semester Examinations,APRIL 2011
COMPUTER ORGANIZATION
Mechatronics

Time: 3 hours | Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks
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1. Explain the following interconnection networks with neat diagram.

   (a) Multistage switching network

   (b) Hyper cube interconnection .   [8+8]

2. Explain in detail the Data transfer and Program control instructions of a computer.
   [16]

3. (a) Explain address sequencing in microprogrammed control unit

   (b) Explain in detail various fields of microinstruction format with diagram. [8+8]

4. What is delayed load ? Give an example program that uses delayed load with three
   segment pipeline.   [16]

5. What are the different ways of representing a signed number? And what is the best
   way of representation and why?   [16]

6. Explain about

   (a) Associative Memory

   (b) Memory mapped I/O.   [8+8]

7. Explain about Asynchronous Data Transfer schems in detail.   [16]

8. (a) Explain Booth's algorithm with its theoretical basis.

   (b) Represent two n-bit unsigned numbers multiplications with a series of n/2-bit
   multiplications.   [8+8]

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Code No: 07A6EC14 | **R07** | **Set No. 1**

III B.Tech II Semester Examinations,APRIL 2011
COMPUTER ORGANIZATION
Mechatronics

Time: 3 hours   Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks
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1. (a) Draw the block diagram of a computer and explain the function of each block.

   (b) Write short note on types of computers.   [8+8]

2. (a) Show the connection model of Memory to the CPU and explain the operation and chip select options?

   (b) Give a Block diagram for a $4M \times 8$ memory using $256K \times 1$ memory chips. [8+8]

3. (a) Explain address sequencing in microprogrammed control unit

   (b) Give the typical horizontal and vertical microinstruction formats.   [8+8]

4. (a) What are the differences between branch instruction, a call subroutine call instruction, and program interrupt?

   (b) Convert the following arithmetic expression into reverse polish notation and show the stack operations for evaluating the numerical result.
   $(3+4) \times [10 \times (2+6)+8]$.   [16]

5. (a) Crossbar switch organization supports "Simultaneous transfer of data from all memory modules". Justify it

   (b) In Omega switching network, "There exists one path from any source to any destination". Justify.   [8+8]

6. (a) Write about instruction format for vector processor.

   (b) Explain the concept of pipeline in calculating inner product.   [8+8]

7. (a) Derive an algorithm in flowchart form for nonrestoring method of fixed- point binary division.

   (b) Explain decimal division algorithm.Design an array multiplier that multiples two 4-bit numbers. Use AND gates and binary adders.   [8+8]

8. (a) Draw the circuit diagram of 4×4 FIFO buses and explain its operation

   (b) Explain about strobe signal and handshaking in detail.   [8+8]

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Code No: 07A6EC14　　　　　　R07　　　　　　Set No. 3

III B.Tech II Semester Examinations,APRIL 2011
COMPUTER ORGANIZATION
Mechatronics

Time: 3 hours　　　　　　　　　　　　　　　　　　　Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks
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1. What is cache memory? Explain the concept of cache coherence in cache memory.
   [16]

2. (a) Draw the diagram for connection between the processor and the memory and explain basic operational concepts of computer.

   (b) Write about bus structures.　　　　　　　　　　　　　　　　[8+8]

3. What is Asynchronous Data Transfer? Explain various methods of asynchronous data transfer with timing diagrams.　　　　　　　　　　　　[16]

4. (a) Give detail picture of pipeline.

   (b) Explain pipeline for floating point addition and subtraction.　　[6+10]

5. A Computer uses RAM chips of 1024 ×1 capacity.

   (a) How many chips are needed, and how should their address lines be connected to provide a memory capacity of 1024 bytes?

   (b) How many chips are needed to provide a memory capacity of 16K bytes? Explain in word how the chips are to be connected to the address bus. . [8+8]

6. (a) What are the major design considerations in microinstruction sequencing?

   (b) Write the fetch routine in the case of microprogrammed control unit?　[8+8]

7. (a) Register A holds the 8-bit binary 11011001. Determine the B operand and the logic micro operation to be performed in order to change the value in A to:

      i. 01101101
      ii. 11111101
      iii. Explain register transfer language. Show how to achieve Inter Register Transfer with examples and block diagram.　　　　　　　[8+8]

8. (a) Consider the decimal numbers 575 and -320, find their sum using BCD adder. Explain the stepwise operation.

   (b) Explain division algorithm for floating-point data.　　　　　　[8+8]

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