Code No: 07A7EC32 **R07** **Set No. 2**

IV B.Tech I Semester Examinations,MAY 2011
VLSI DESIGN
Common to Electronics And Computer Engineering, Electronics And Instrumentation Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. What is a stick diagram and explain about different symbols used for components in stick diagram with suitable example. [16]

2. (a) Discuss the main processing steps in a CMOS N - well fabrication.
   (b) Explain twin tub structure, mentioning its merits and demerits. [8+8]

3. (a) Explain different forms of pull ups used as load, in CMOS and in enhancement & depletion modes of NMOS.
   (b) Determine the pull up to pull down ratio of an nMOS inverter driven by another nMOS transistor. [8+8]

4. What is an LUT? Explain how an 4 to 1 multiplexer is implemented using LUT? [16]

5. Explain the scan-path design technique used to test sequential circuits in detail. [16]

6. (a) Compare the behavioral and structural styles of VHDL with example.
   (b) Explain the method of Binary composition for chip routing with suitable example. [8+8]

7. (a) Compare different types of CMOS subsystem Adders.
   (b) Draw the mask layout for 6 transistor static RAM used in ASIC memories. [8+8]

8. (a) Define the following and explain the significance of each term in VLSI circuits
      i. Fan in
      ii. Fan out
      iii. Stage Ratio.
   (b) Write the equation for
      i. t_{dr}
      ii. t_{df}

   of m input NAND gate. [4+4+4+2+2]

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Code No: 07A7EC32 **R07** **Set No. 4**

IV B.Tech I Semester Examinations,MAY 2011
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Explain briefly the CMOS system design based on the data path operators, memory elements, control structures and I/O cells with suitable examples. [16]
2. (a) Show that the pull up to pull down ratio of an nMOS inverter driven by another nMOS inverter is 4:1.
   (b) Define threshold voltage of a MOS device and explain its significance? [10+6]
3. Explain the following with respect to CMOS testing: [4×4=16]
   (a) ATPG
   (b) Fault simulation
   (c) Statistical Fault Analysis
   (d) Fault Sampling.
4. Draw the structure of PLA and how the clocks are selected in PLA such that the OR plane outputs must be captured before the AND plane pre-charges ? What are the applications of it? [16]
5. Describe the following briefly:
   (a) Cascaded inverters as drivers.
   (b) Super buffers.
   (c) BiCMOS drivers. [8+4+4]
6. (a) What is Selected Signal Assignment Statement? Write a syntax in VHDL.
   (b) Explain how the timing analyzers are used to verify the functionality of CMOS chip. [8+8]
7. Briefly discuss the limits of scaling. Why scaling is necessary for VLSI circuits? [16]
8. Describe the X-ray lithography with necessary diagrams. [16]

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Code No: 07A7EC32 **R07** **Set No. 1**

IV B.Tech I Semester Examinations,MAY 2011
VLSI DESIGN
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Define and explain the following:
   i. Sheet resistance concept applied to MOS transistors and inverters.
   ii. Standard unit of capacitance.
   (b) Explain the requirement and functioning of a delay unit. [4+4+8]
2. (a) What are the main categories of testing? Explain these with examples.
   (b) Draw the block level implementation of a polarity hold SRL and explain its working.
   (c) How ROM memories can be tested? [6+6+4]
3. Mention the properties of oxidation, explaining thermal oxidation technique. [16]
4. (a) Draw and explain the schematic of Pseudo-nMOS comparator.
   (b) Draw and explain the structure of multiplier which computes the partial products in a radix-2 manner. [8+8]
5. (a) Design stick diagram and layout for two input nMOS NOR gate.
   (b) Draw the stick diagram and layout for two input CMOS NOR gate. [8+8]
6. (a) What are the differences between a gate array chip and standard-cell chip? What benefits does each implementation style have?
   (b) Write the equations for a full adder in SOP form. Sketch a 3-input, 2- output PLA implementing this logic. [8+8]
7. (a) A CMOS inverter is built in a process where k'n=100μA/V^2, V_{tn}=+0.7V, k'_p =42 μA/V^2 , V_{tp}=-0.8V, and a power supply of V_{DD} =3.33V is used .Find mid point voltage V_M if $(W/L)_n$ =10 and $(W/L)_p$= 14.
   (b) Discuss the CMOS invertors transfer characteristics. [8+8]
8. (a) Write a VHDL program for 7-sengment display decoder.
   (b) What are the basic sources of errors in CMOS circuits and how these are tested? Give name of such a simulator. [8+8]

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Code No: 07A7EC32 **R07** **Set No. 3**

IV B.Tech I Semester Examinations,MAY 2011
VLSI DESIGN
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) What are the draw backs of PLAs? How PLAs are used to implement combinational and sequential logic circuits?
   (b) Draw the schematic of CPLD and compare it with FPGA. [8+8]
2. (a) Explain the CMOS system design based on the control structures with suitable example.
   (b) What are the different types of Memory elements? Compare them with respect to CMOS design. [8+8]
3. (a) What are the advantages of BICMOS Technology over CMOS Technology?
   (b) Explain how a bipolar NPN transistor is included in N well CMOS processing. Draw the cross section of BICMOS transistor. [4+12]
4. (a) What is meant by enumeration type of data and give some example for it?
   (b) What are the different Libraries used in VHDL? Write the syntax to load it.
   (c) Explain how the delay of a statement is related to simulation and synthesis. [6+6+4]
5. (a) What is BIST? Explain in detail.
   (b) Write the advantages of BIST. [10+6]
6. Design a stick diagram and layout diagram for the CMOS logic shown below $Y = \overline{(A+B)(C+D)}$. [16]
7. Two nMOS inverters are cascaded to drive a capacitive load C_L=16 $\square C_g$. Calculate the pair delay (V_{in} to V_{out}) in terms of τ for the inverter geometry indicated in figure 7. What are the ratios of each inverter? If strays and wiring are allowed for,it would be reasonable to increase the capacitance to ground across the output of each inverter by 4 $\square C_g$. What is the pair delayallowing for strays? Assume a suitable value for τ and evaluate this pair delay. [16]
   Inverter 1 $L_{pu} = 16\lambda$, $W_{pu} = 2\lambda$, $L_{pd} = 2\lambda$,$W_{pd} = 2\lambda$
   Inverter 2 $L_{pu} = 2\lambda$,$W_{pu} = 2\lambda$, $L_{pd} = 2\lambda$, $W_{pd} = 8\lambda$

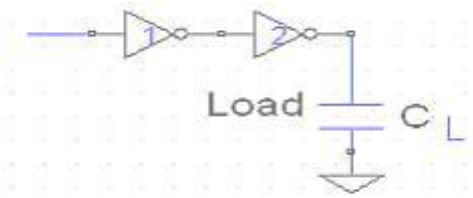

Figure 7

8. (a) clearly explain about channel length modulation of the MOSFET.
   (b) Discuss the effects of parasitic capacitances between gate and source/drain overlap regions of MOS transistors. [8+8]

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