Code No: 07A80305 **R07** **Set No. 2**

IV B.Tech II Semester Examinations,APRIL 2011
COMPUTER ORGANIZATION AND ARCHITECTURE
Common to Mechanical Engineering, Automobile Engineering
Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Show the value of all bits of a 12-bit register that hold the number equivalent to decimal 215 in:
   (a) Binary
   (b) Binary-coded octal
   (c) Binary - coded hexadecimal. [16]
2. (a) Consider a single-transistor dynamic memory cell. Assume that C = 50 fento-farads and the leakage current through the transistor is about 9 pico amperes. The voltage across the capacitor when it is fully charged is equal to 4.5V. The cell must be refreshed before this voltage drops below 3V. Estimate the minimum refresh rate.
   (b) Discuss in detail about various features of ROM, PROM and EPROM.[6+10]
3. (a) Define the term Parallel Processing and explain the need of it with an example.
   (b) Discuss in detail about the four major groups according to the Flynn's classification with respect to Parallel Processing. [8+8]
4. (a) What is Symbolic micro program, explain?
   (b) Taking an example design a control unit. [8+8]
5. (a) Discuss in detail about the various processes involved in Multiport memory with a neat block diagram consisting of inter connections for four CPUs and four memory modules.
   (b) The 8×8 omega switching network has three stages with four switches in each stage, for a total of 12 switches. How many stages amd switches per stage are needed in an n × n omega switching network? [10+6]
6. (a) Explain in detail about the operation of a universal asynchronous receiver transmitter with a neat diagram.
   (b) Draw the timing diagram and expalin about asynchronous serial transmission. [11+5]
7. The content of PC in the basic computer is 3AF (all numbers are in hexadecimal). The content of AC is 7EC3. The content of memory at address 3AF is 932E. The content of memory at address 32E is 09AC. The content of memory at address 9AC is 8B9F.

(a) What is the instruction that will be fetched and executed next?

(b) Show the binary operation that will be performed in the AC when the instruction is executed.

(c) Give the contents of registers PC, AR, DR, AC and IR in hexadecimal and the values of E, I and the sequence counter SC in binary at the end of the instruction cycle. [16]

8. Given the 16 bit value 1001101011001101. What operation must be performed in order to?

(a) Clear to 0 the first eight bits

(b) Set to 1 the last eight bits

(c) Complement the middle eight bits. [16]

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1. Differentiate the RISC and CISC processor characteristics. [16]

2. (a) What is the function of a Multiprocessor system and list out the various characteristics of Multiprocessors?
   (b) Explain how the Multiprocessors are classified based on way their memory organization. [10+6]

3. (a) Explain asynchronous data transfer modes.
   (b) Identify the standard binary code for the alphanumeric characters and explain about them with examples. [9+7]

4. With respect to the performance considerations, discuss about the following:
   (a) Write buffer
   (b) Prefetching
   (c) Lock up-Free cache. [5+6+5]

5. (a) Draw and explain a space-time diagram for a six-segment pipeline showing the time it takes to process eight tasks.
   (b) With an example, demonstrate the pipeline organization. [8+8]

6. (a) Explain the stages of pipelining in detail.
   (b) What is micro program sequencer in micro programmed control organization? [8+8]

7. A basic computer is starting to perform instruction ADD 100 I. Given preconditions are (values are hex decimals):
   - PC = 190
   - AC = 3
   - M[100] = 200
   - M[200] = fffe

   (a) Describe what happens during the instruction cycle. Include all phases from fetch to execute.
   (b) If an I/O device requests for an interrupt during the instruction cycle, what happens? Describe the events starting from the fetch phase of the current instruction until the machine is ready to branch to the interrupt subroutine of the I/O device. [16]

8. Derive the circuits for a 3-bit parity generator and 4bit parity checker using an even parity bit. [16]

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Code No: 07A80305 **R07** **Set No. 1**

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COMPUTER ORGANIZATION AND ARCHITECTURE
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Answer any FIVE Questions
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1. (a) 'Parallel Processing can be viewed from various levels of complexity'. Explain the statement with necessary reasons.
   (b) List out and explain various advantages of a parallel processing system. [6+10]
2. (a) With a neat diagram, discuss in detail about the possible address assignment for a byte-addressable 32-bit computer.
   (b) Draw the block diagram showing various connections of the main memory to the CPU. Also, explain about issues related to their bus structures. [7+9]
3. (a) How many characters per second can be transmitted over a 1200-baud line in each of the following modes? (Assume a character code of eight bits):
      i. Synchronous serial transmission
      ii. Asynchronous serial transmission with two stop bits
      iii. Asynchronous serial transmission with one stop bit.
   (b) List out the salient features of First-In, First-Out Buffer. [6+10]
4. Show the bit configuration of a 24-bit register when its content represents the decimal equivalent of 400:
   (a) in binary
   (b) in BCD
   (c) in ASCII using eight bits with even parity. [16]
5. (a) What is the difference between microprocessor and micro program?Is it possible to design a microprocessor without a micro program? Are all micro programmed computers also microprocessor?
   (b) Explain the difference between hardwired control and micro programmed control. Is it possible to have a hardwired control associated with a control memory? [8+8]
6. (a) What are the different addressing modes, explain in detail with example?
   (b) What are Berkeley RISC I instruction formats, explain? [8+8]
7. The following control inputs are active in the bus system, For each case, specify the register transfer that will be executed during the next clock transition. [16]

	S2	S1	S0	value S	LD(x)	Memory	Adder
a)	1	1	1	=7	IR	READ	-
b)	1	1	0	=6	PC	-	-
c)	1	0	0	=4	DR	WRITE	-
d)	0	0	0	=0	AC	-	ADD

8. (a) Draw a diagram showing the structure of a four-dimentional hypercube network. List all the paths available from node 7 to node 9 that use the minimum number of intermediate nodes.

   (b) Compare parallel and serial arbitration procedure? [10+6]

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Code No: 07A80305 **R07** **Set No. 3**

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1. (a) Define: i) Micro operation ii) Micro instructions iii) Micro program iv) Micro code.
   (b) Explain how the mapping from an instruction code to microinstruction address can be done by means of a read-only memory. [8+8]

2. (a) What are the functions of an array processor?
   (b) Differentiate between Attached and SIMD Array Processors with respect to any six parameters.
   (c) Compare Vector and Array Processings. [4+6+6]

3. Design a 4bit combinational circuit decrementer using four full adder circuits. [16]

4. (a) Explain in detail about the impact of the cache on the overall performance of the computer with respect to hit rate and hiss rate.
   (b) List out the salient features of memory inter learning. [12+4]

5. (a) What are different types of memories, which is the fastest and slowest of all, which is cheapest and which is costly, memory.
   (b) Is a WLAN connectivity an IO system, if yes which part of memory is associated to this interface. [8+8]

6. Show the bit configuration of a 24-bit register when its content represents the decimal equivalent of 295:
   (a) in binary
   (b) in BCD
   (c) in ASCII using eight bits with even parity. [16]

7. (a) Give at least six status conditions for the setting of individual bits in the status register of an asynchronous communication interface.
   (b) How many bits are there in the transmitter shift register of a UART when the interface is attached to a terminal that needs one stop bit? List the bits in the shift register when the letter W is transmitted using ASCII with even parity. [6+12]

8. (a) Bringout the differences between the cross bar switch and multistage switching networks.

(b) Construct a diagram for a 4 × 4 omega switching network. Show the switch setting required to connect input 3 to output 1. [8+8]

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