

Code No: 07A80405

R07**Set No. 2**

IV B.Tech II Semester Examinations, APRIL 2011

DIGITAL DESIGN THROUGH VERILOG**Common to Bio-Medical Engineering, Electronics And Computer
Engineering, Electronics And Communication Engineering****Time: 3 hours****Max Marks: 80****Answer any FIVE Questions
All Questions carry equal marks**

1. (a) Classify and explain strengths and contention resolution?
(b) Design module to illustrate use of the wand-type net and test bench with stimulation results? [8+8]
2. (a) Design half-adder module with time delay assignment through parameter declaration.
(b) Write Test bench, simulation results for the above. [8+8]
3. Explain the following terms.
(a) Simulation
(b) Synthesis
(c) Implementation
(d) HDLS [16]
4. (a) Design verilog code of OR gate using for and disable.
(b) Write simulation results of above question with explanation. [8+8]
5. Design HDL module for UART Transmitter. [16]
6. (a) Design a verilog module of a 4 bit bus switcher at the data flow level.
(b) Design verilog module of an edge triggered flip-flop built with the latch at the data flow level. [8+8]
7. Explain one hot state assignment with example. [16]
8. (a) Draw the block diagram for a divider that divides an 8-bit dividend by a 5-bit divisor to give a 3-bit quotient. The dividend register should be loaded when St=1.
(b) Draw an SM chart for the control unit. [8+8]

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1. (a) Design CMOS flipflop.
(b) Design verilog module for CMOS flipflop. [8+8]
2. (a) Define While loop, write syntax with flow chart.
(b) Explain for loop example with verilog code. [8+8]
3. (a) Design a D flip flop using NAND gates.
(b) Write a verilog code for D flip flop using NAND gates. [8+8]
4. (a) Explain the linked state machines.
(b) Explain the linked SM charts to Dice game. [8+8]
5. (a) Write about \$ readmemb with example.
(b) Write value change dump file. [8+8]
6. Explain UART Receiver with SM Chart. [16]
7. Explain about flex 10k embedded array block. [16]
8. (a) Explain simple latch with verilog module?
(b) Explain RS Flip-flop with verilog module and Test Bench? [8+8]

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R07**Set No. 1**

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1. (a) Explain asymmetric sequence generator with example.
(b) Explain automatic (re-entrant) tasks with example. [8+8]
2. (a) Design SM chart for Dice game test.
(b) Write Tester for Dice game (HDL module). [8+8]
3. (a) Classify delays and explain?
(b) Explain delays with Tristate Gates? [8+8]
4. (a) Design Up counter coding procedural assignment.
(b) Write Up counter test bench, simulation results. [8+8]
5. Explain UART Design:
(a) Serial Data Transmission.
(b) Standard Serial Data format.
(c) Block diagram. [16]
6. Explain signal paths within adder subtractor logic cell. [16]
7. (a) Explain clocked RS Flip-flop verilog module and Test Bench?
(b) Write about and differences scalars and vectors in verilog module, with examples? [8+8]
8. (a) Design half adder using CMOS switches.
(b) Write the verilog code for half adder using CMOS switches. [8+8]

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1. (a) Design a JK flip flop using NAND gates.
(b) Write a verilog code for JK flip flop using NAND gates. [8+8]
2. (a) Explain module with an example using verilog code?
(b) Explain port Declaration with an example using verilog code? [8+8]
3. (a) Explain edge sensitive path using an example.
(b) Explain over riding parameters. [8+8]
4. Explain UART Transmission with SM Chart. [16]
5. (a) Explain NMOS enhancement with conditions.
(b) Write about Basic switch primitives. [8+8]
6. Explain parallel adder-subtractor with logic cell. [16]
7. (a) Write a verilog module for a rudimentary serial transmitter module.
(b) Explain Multiple Always Blocks. [8+8]
8. (a) Construct an PLA and D-flip flop equivalent to the following state table. Test only one variable in each decision box. Try to minimize the number of decision boxes.
(b) Write a VHDL description of the state machine based on the PLA and D-flip flop. [8+8]

Present State	Next state				Output Z1Z2			
	X1X2=00	01	10	11	X1X2=00	01	10	11
S0	S3	S2	S1	S0	00	10	11	01
S1	S0	S1	S2	S3	10	10	11	11
S2	S3	S0	S1	S1	00	10	11	01
S3	S2	S2	S1	S0	00	00	01	01
