Code No. M0523   **R07**   **Set No.1**

IV B.Tech I Semester Supplementary Examinations, February, 2012
ADVANCED COMPUTER ARCHITECTURE
(Computer Science and Engineering)

Time: 3 hours   **Max. Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks
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1. a) What are the rapidly changing technologies that may shape the design of a computer?
   b) What are the major factors that influence the cost of a computer and how these factors are changing over time?
   c) Define Amdahl's law? How much speed can be enhanced by replacing the system with a new processor that is 100 times faster than the old. Assume the original processor is busy with computation 50% of the time and the remaining time is waiting for I/O devices.

2. a) What are the data addressing modes that are considered to be very popular? Explain Auto increment and Auto decrement addressing with examples.
   b) Name four important features where the register indirect jumps are useful.
   c) What is the impact of compiler technology on the computer architect's decisions?

3. What is the major hurdle of pipelining? How do they reduce the performance? What are the techniques to be used to improve the performance?

4. What are the five primary approaches, in use, for multiple issue processors? Give the primary characteristics that distinguish them.

5. a) What are the parameters used to describe the performance of cache? Explain.
   b) Summarize the techniques used for cache optimizations and estimate the impact on the parameters that characterizes its performance.

6. a) What is multiprocessor cache coherence?
   b) What are the limitations in symmetric shared multiprocessors?
   c) Explain the basic synchronization mechanism for multi processors.

7. a) Give the different characteristics of transaction processing benchmarks for I/O systems.
   b) Describe cluster architecture.

8. Write short notes on the following.
   a) RAID and its performance
   b) Practical issues in interconnection networks.

Code No. M0523   **R07**   **Set No.2**

IV B.Tech I Semester Supplementary Examinations, February, 2012
ADVANCED COMPUTER ARCHITECTURE
(Computer Science and Engineering)

Time: 3 hours   **Max. Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks
*****

1 a) What are the relative improvements in bandwidth and latency in technology milestones for microprocessors, memory, networks, and disks?
   b) What is dependability? What are the factors that influence the system to be very dependable?
   c) What are the parameters that dictate the processor performance? Explain.

2 a) How instruction set architectures are classified? Give their relative merits and demerits?
   b) How to encode the addressing modes with operations? What are the factors to be considered in decoding mechanism ?
   c) What are the guidelines that make the design of compiler to be easy and efficient?

3 a) What are control hazards? How advanced branch production reduces the branch costs?
   b) What are limitations of instruction level parallelism?
   c) What are the features of hardware based speculation to overcome the control dependences?

4 a) How VLIW approach improves the performance of pipelines?
   b) Name three primary dynamic approaches, that are hardware based, for hazard detection to instruction level parallelism? Give their primary characteristics. How do you differentiate among them?

5 How use of virtual machine has gained popularity? How the processes are protected from each other through virtual machines?

6 a) Differentiate between centralized shared memory multiprocessors and distributed memory multiprocessors.
   b) What is multi threading? How do you define thread level parallelism? How spin locks be implemented using coherence mechanism?

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Code No. M0523 **R07** Set No.2

7 a) How an I/O system is designed and evaluated?
   b) Discuss performance issues related to I/O systems.

8 Write short notes on the following.
        a) Hardware multithreading and its performance.
        b) Role of compiler in encoding an instruction set.

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Code No. M0523

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Set No.3

IV B.Tech I Semester Supplementary Examinations, February, 2012
ADVANCED COMPUTER ARCHITECTURE
(Computer Science and Engineering)

Time: 3 hours **Max. Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks
*****

1. a) Describe the performance milestones of microprocessors, memory, networks and disks.
    b) How the performance of a system can be measured and reported?
    c) How speed up can be achieved by making an enhancement to a computer?

2. a) Explain the displacement addressing mode with an example and give its usefulness.
    b) What are the major methods for evaluating branch conditions? Give three advantages and disadvantages.
    c) What are the optimizations that can be performed by modern compilers ?

3. a) What are data hazards that are noticed in instructing level parallelism? Explain dynamic scheduling for overcoming these   hazards.
    b) How high performance instruction delivery without hazards, is possible in instruction level parallelism?

4. a) Explain static branch prediction? What is the advantage of using this?
    b) What are the relative merits and demerits of adapting software and hardware supports for improving the performance of pipelines?

5. a) What are the causes for high miss rates in cache organization? What are the six basic cache optimizations?
    b) How architecture supports for protecting processes from each other via virtual memory?

6. a) Describe Flynn classification of parallel architectures.
    b) What is multi threading? How does it improve the performance of multiprocessors?
    c) What is cache coherence? Name the methods used to take care of coherence problems.

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R07

Set No.3

7. a) Name any three I/O benchmarks along with their throughput metrics and time restrictions.

   b) How the performance and reliability of I/O systems are improved with the use of RAID?

8. Write short notes on the following.

   a) Message passing multiprocessors.

   b) Quantities measures for performance of computers.

Code No. M0523   **R07**   **Set No.4**

IV B.Tech I Semester Supplementary Examinations, February, 2012
ADVANCED COMPUTER ARCHITECTURE
(Computer Science and Engineering)

Time: 3 hours   **Max. Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks
*****

1. a) What are trends in power in the integrated circuits for exploration of better computing machines?

    b) What are benchmarks? What is the role of benchmarks in measuring performance of computer systems?

    c) What are the guidelines and principles that are useful in the design and analysis of computers?

2. a) What are the data addressing modes that are found to be very efficient for dealing control flow instruction? Explain.

    b) How instructions are encoded into a binary representation? Does this representation has any bearing on the performance of the computer? What is the competing forces when encoding a instruction set?

3. a) What is a pipeline? What are data dependences and hazards? Explain

    b) What are the key ideas of hardware based speculation? What is the purpose of using recorder buffers?

4. a) Differentiate between software verses hardware solutions for hazard detection.

    b) How the hardware support improves the instruction level parallelism at compiler time?

5. Name ten advanced optimizations of cache performance and explain each of the techniques.

6. a) What are multiprocessors? How they are connected using an interconnection network?

    b) Differentiate between instruction level parallelism and thread level parallelism.

    c) What is synchronization? Why synchronization mechanism is needed for multiprocessor systems?

    d) What are the possible messages sent among the processors to maintain coherence in multiprocessors?

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Code No. M0523 **R07** Set No.4

7. a) What is the general approach to design an I/O system?
   b) What are the errors and types of failures that are usually noticed in I/O systems?
   c) What are the practical issues in designing interconnection networks?

8. Write short notes on
   a) Designing a cluster.
   b) Amdahl's law and its limitations.