Code No: M0523/R07 **Set No. 1**

IV B.Tech I Semester Supplementary Examinations, March 2013
ADVANCED COMPUTER ARCHITECTURE
(Computer Science & Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain Amdhal's law?
   (b) Find the number of dies for 30 cm wafer for a die that is 0.7cm on a side.[8+8]
2. Give a brief account on data sizes and types. [16]
3. Explain the effect of window size on each application with the help of neat diagram. [16]
4. Write notes on superscalar processors. [16]
5. (a) What do you mean by the term 'cache'? Explain its usage with examples.
   (b) On what factors the time required for 'cache miss'depends. Explain. [8+8]
6. (a) Suppose there are 10 processors on a bus that each try to lock a variable simultaneously. Assume that each bus transaction [read miss or write miss] is 100 clock cycles long. You can ignore the time of the actual read or write of a clock held in the cache, as well as the time the lock is held. Determine the number of bus transactions required for all 10 processors to acquire the lock, assuming they are all spinning when the lock is released at time is 0.about how long will it take to process the 10requests? Assume that the bus is totally fair so that every pending request is serviced before a new request and that the processors are equally fast.
   (b) What is meant by barrier? How can it be implemented? [8+8]
7. (a) Suppose an IO system with a single disk gets on average 50 IO requests per sec. Assume the average time for the disk to service an IO request is 10ms. What is utilization of an IO system?
   (b) Write about the errors and failures in Berkeley's tertiary disk. [8+8]
8. (a) What will determine latency and performance: the interfaces to the network or the core performance: the interfaces to the network or the core network fabric?
   (b) Draw the diagram of Hyper cube with 16 nodes? Explain. [8+8]

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Code No: M0523/R07 **Set No. 2**

IV B.Tech I Semester Supplementary Examinations, March 2013
ADVANCED COMPUTER ARCHITECTURE
(Computer Science & Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain Amdhal's law?
   (b) Find the number of dies for 30 cm wafer for a die that is 0.7cm on a side.[8+8]
2. Give a brief account on streaming SIMD extension (SSE). [16]
3. List out the three models of memory alias analysis and explain. [16]
4. What is loop unrolling? What are the three different limits of loop unrolling? Explain [16]
5. (a) Write about cache and performance.
   (b) Calculate the cpu execution time for a computer with clock cycles per instruction as 1.0 when all memory accesses hit in the cache.The only data accesses or loads and stores, and these total 50% of the instructions. If the miss penalty is 25 clock cycles and the miss rate is 2%,how much faster would the computer be if all instructions were cache hits? [8+8]
6. (a) How to prevent coherence problem in a scalable multiprocessor supporting shared memory? what are the disadvantages?
   (b) Discuss about directory protocol. [8+8]
7. (a) What is the meant by flash memory and explain? What is the difference between the flash memory and PROM?
   (b) Compare the times to read and write a 64KB block to a flash memory and magnetic disk. For flash assume it takes 65ns to read 1byte, 1.5μs to write 1byte, and 5ms to erase 4KB. Assume the measure seek time is $1/3^{rd}$ of the calculated average, the controller overhead is .1ms and the data stored in the outer tracks ,give it the faster transfer rates. [8+8]
8. Explain [4×4]
   (a) Switches
   (b) Circuit switching
   (c) Worm whole routing
   (d) Destination based routing.

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Code No: M0523/R07 **Set No. 3**

IV B.Tech I Semester Supplementary Examinations, March 2013
ADVANCED COMPUTER ARCHITECTURE
(Computer Science & Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Write short notes on:
   (a) TCP Benchmark.
   (b) Learning curves. [8+8]
2. (a) Write detailed notes on memory-memory architecture.
   (b) Brifly etailed explain about position independence? [12+4]
3. Write notes on finite registers. [16]
4. What are the basic compiler techniques for exposing ILP? [16]
5. (a) Give the types of "Conflict misses".
   (b) Which principle of locality does the first miss rate reduction technique address? Explain why? [8+8]
6. (a) On what problem sizes the performance of scientific technical workload is measured. Explain.
   (b) What factors contribute to L3 cache miss rate and how do they change as the L3 cache grows? [8+8]
7. (a) Define dependability. How can we improve dependability? Explain.
   (b) Write briefly about the benchmarks of dependability and availability. [8+8]
8. Discuss about the practical issues for commercial interconnection networks? [16]

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Code No: M0523/R07 **Set No. 4**

IV B.Tech I Semester Supplementary Examinations, March 2013
ADVANCED COMPUTER ARCHITECTURE
(Computer Science & Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Explain measuring and Reporting performance in computer design. [16]
2. Give a detailed note on graph coloring with appropriate examples? [16]
3. Give a brief account on dynamic scheduling. What are its advantages and disadvantages? [16]
4. Explain pipeline scheduling in detail. [16]
5. (a) Explain how to improve cache performance?
   (b) Assume the cache miss penalty is 100 clock cycles and all instructions normally take 1.0 clock cycles [ignoring memory stalls]. Assume the average miss rate is 2%, there is an average of 1.5 memory references for instruction, and the average number of cache misses per 1000 instructions is 30. What is the impact on performance when behavior of the cache is included? Calculate the impact using both misses per instruction and miss rate. [8+8]
6. (a) On what factors does Flynn's classifications of computer is based. Explain the categories.
   (b) What do you mean by thread level parallelism? [8+8]
7. (a) Give the classification of faults and mention their cause.
   (b) Define fault, error, failure. What is the variation among them?
   (c) Define reliability, availability, and dependability. [6+5+5]
8. What is a cluster? Explain about the designing of a cluster with an example. [16]

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