Code No: M0523/R07 **Set No. 1**

IV B.Tech I Semester Regular Examinations, November 2012
ADVANCED COMPUTER ARCHITECTURE
(Computer Science & Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Define learning curve. Explain?
   (b) Explain the need for parallelism. [8+8]
2. Discuss the characterstics of RISC? How does it differ from CISC? [16]
3. Write notes on finite registers. [16]
4. Write notes on superscalar processors. [16]
5. (a) What is meant by dirty bit? What is its use in cache?
   (b) Compare and contrast write through and write back policies.
   (c) what is done on a "write miss"? [5+6+5]
6. (a) Write about the hardware primitives for synchronization.
   (b) Explain about spin locks with an examples. [8+8]
7. Write about
   (a) Memory mapped IO
   (b) Interrupt driven IO
   (c) Polling. [6+6+4]
8. (a) What are the major functions of an I/O module?
   (b) What is the difference between memory mapped I/O and isolated I/O?
   (c) What is meant by direct memory access? [6+5+5]

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Code No: M0523/R07 **Set No. 2**

IV B.Tech I Semester Regular Examinations, November 2012
ADVANCED COMPUTER ARCHITECTURE
(Computer Science & Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Write short notes on:
   (a) Transaction processing Benchmark.
   (b) Server Benchmark [8+8]
2. (a) What are the reasons for emergence of general purpose registers?
   (b) Distinguish between little endian and big endian format? [8+8]
3. Explain data dependent hazard with example? [16]
4. Explain with example loop unrolling? [16]
5. (a) Explain how to improve cache performance?
   (b) Assume the cache miss penalty is 100 clock cycles and all instructions normally take 1.0 clock cycles [ignoring memory stalls]. Assume the average miss rate is 2%, there is an average of 1.5 memory references for instruction, and the average number of cache misses per 1000 instructions is 30. What is the impact on performance when behavior of the cache is included? Calculate the impact using both misses per instruction and miss rate. [8+8]
6. (a) Suppose there are 10 processors on a bus that each try to lock a variable simultaneously. Assume that each bus transaction [read miss or write miss] is 100 clock cycles long. You can ignore the time of the actual read or write of a clock held in the cache, as well as the time the lock is held. Determine the number of bus transactions required for all 10 processors to acquire the lock, assuming they are all spinning when the lock is released at time is 0.about how long will it take to process the 10requests? Assume that the bus is totally fair so that every pending request is serviced before a new request and that the processors are equally fast.
   (b) What is meant by barrier? How can it be implemented? [8+8]
7. (a) Compare the RAID levels and their fault tolerance and overhead in the redundancy disk.
   (b) Write a note on the following:
      i. Average rotation time
      ii. Seek time
      iii. Constant bit density. [7+9]

Code No: M0523/R07 **Set No. 2**

8. (a) What is the natural size of message. Explain how a message size is important in getting full benefits of fast network?
   (b) Which media are available to connect computing together? [8+8]

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Code No: M0523/R07 **Set No. 3**

IV B.Tech I Semester Regular Examinations, November 2012
ADVANCED COMPUTER ARCHITECTURE
(Computer Science & Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Write short notes on
   (a) learning curves.
   (b) Amdhal's law. [8+8]
2. (a) Define little endian format.
   (b) Discuss in detail about the instructions used for flow control. [4+12]
3. Explain data dependent hazard with example? [16]
4. Write notes on multiple issues: the VLIW approach. [16]
5. Compare the relative merits of the four cache memory organizations. [16]
6. (a) What is multiprocessor cache coherence?
   (b) Explain about multiprogramming and OS workload. [8+8]
7. (a) What is the average time to read or write a 512 bytes sector for a disk? The advertised average seek time is 5ms, the transfer rate is 40MB/sec, it rotates at 10,000RPM, and the controller overhead is 0.1ms. Assume the disk is idle so that there is no queuing delay. In addition, calculate the time assuming the advertised seek time is 3 times longer than the measured seek time.
   (b) Write about
      i. Optical Disk
      ii. Magnetic Tapes. [8+8]
8. Write about
   (a) Ethernet
   (b) ATM. [8+8]

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Code No: M0523/R07 **Set No. 4**

IV B.Tech I Semester Regular Examinations, November 2012
ADVANCED COMPUTER ARCHITECTURE
(Computer Science & Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain Amdhal's law?
   (b) Find the number of dies for 30 cm wafer for a die that is 0.7cm on a side. [8+8]
2. What are the different properties that have to be taken into account to write compiler that will generate efficient and correct code? Explain. [16]
3. Explain data dependent hazard with example? [16]
4. What is meant by trace scheduling? Explain in detail? [16]
5. Compare the relative merits of the four cache memory organizations. [16]
6. (a) Write about the hardware primitives for synchronization.
   (b) Explain about spin locks with an examples. [8+8]
7. (a) Define throughput. Discuss how IO performance limits system performance and effectiveness.
   (b) Write about the characteristics of the magnetic disks. [8+8]
8. Discuss about the practical issues for commercial interconnection networks? [16]

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