Code: 9A05704

R09

B.Tech IV Year II Semester (R09) Advanced Supplementary Examinations, July 2013
ADVANCED COMPUTER ARCHITECTURE
(Electronics and Computer Engineering)

Time: 3 hours
Max. Marks: 70

Answer any FIVE questions
All questions carry equal marks
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1   (a)   Show the register to register architecture of a vector super computer. Briefly describe about it.
    (b)   Describe the topologies of static connection networks in terms of network parameters and relative merits in relation to communication and scalability.

2   (a)   Describe about any one speedup performance model.
    (b)   What are the two architectural models of a basic scalar computer system? Write in detail about them.

3   (a)   Show two address formats for memory interleaving, in memory organizations with diagrams.
    (b)   Discuss about a pipelined processor with multiple functional units and distributed reservation stations with diagram.

4   (a)   How will be the I/O operation cause a cache inconsistency? Suggest solution.
    (b)   How X-Y routing on a 2D-mesh connected multicomputer work? Demonstrate.

5   (a)   Draw the DEC VAX 9000 system architecture and vector processor design.
    (b)   Write about the functional architectures of control processors and the processing node in CM-5.

6   (a)   Explain four of the context switching policies.
    (b)   How will the data flow architecture work?

7   (a)   Demonstrate operand forwarding with examples.
    (b)   How much effective is the branch prediction in instruction level parallelism?

8   (a)   What are the various forms of parallelism? Brief about them.
    (b)   What is VLIW? Explain.

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