Code: 9A05704

1

B.Tech IV Year II Semester (R09) Regular Examinations, March/April 2013

ADVANCED COMPUTER ARCHITECTURE

(Electronics & Computer Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions.
All questions carry equal marks.

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1 (a) Discuss about the evolution of computer architectures.
(b) What are the system attributes and specify how the performance factors are influenced by system attributes?

2 (a) State and explain Gustafson's law for scaled problems.
(b) Write down the differences between RISC and CISC architectures.

3 (a) Explain different bus systems with relevant diagram.
(b) Explain four-way sector mapping cache organization.

4 What is cache coherency? Explain various cache coherence protocols that cope up with the multi cache inconsistency problems.

5 (a) Define vector processor. List and explain various types of vector instructions.
(b) Draw and explain the CM-5 network architecture.

6 (a) What are data flow graphs and data flow machines? Explain the ETL EM-4 data flow architecture.
(b) Distinguish between the following:
(i) Static data flow computers and dynamic data flow computers.
(ii) Fine-grain parallelism and coarse-grain parallelism.

7 (a) Discuss the basic design issues of ILP.
(b) What is a basic block? Explain data dependences and control dependences with relevant example.

8 Explain the following terms:
(a) Parallel algorithms.
(b) Stream processing.

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1 (a) Explain briefly about shared and distributed memory multiprocessors.
(b) Discuss about PRAM and VLSI models.

2 Write down the applications of parallel processing also explain each application with relevant examples.

3 Explain the following briefly:
(a) Shared memory organization.
(b) Sequential and weak consistency models.

4 Describe various message-passage mechanisms of parallel and scalable architecture.

5 (a) Explain the vector registers in Cray and Fujitsu machines with neat diagram.
(b) Write down the performance-directed design rules of multivector multiprocessors.

6 (a) Describe briefly about fine-grain parallelism.
(b) Draw an explain the schematic block diagram and chip floor plan of MDP architecture.

7 (a) State and explain Tomasulo's algorithm and RAW dependence with an example.
(b) What is branch prediction? Explain its importance in multiple issue processors.

8 (a) Discuss briefly about structure parallelism and instruction level parallelism.
(b) Explain how to evaluate double integration using a simple parallel algorithm.

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1 Discuss about various conditions of parallelism with an example of each.

2 (a) Describe the memory hierarchy with a neat diagram.
(b) Explain address translation mechanism using TLB in virtual memories.

3 (a) Explain the differences between linear and non-linear pipeline processors.
(b) Discuss the dynamic instruction scheduling with an example.

4 (a) Explain the hierarchical bus systems architecture with a neat diagram.
(b) What are the limitations of cross bar switch?

5 (a) Draw and explain the schematic block diagram of Y-MP 816 system.
(b) Write a short note on vector-loops.

6 (a) Discuss various prefetching techniques along with their benefits and benchmark results.
(b) Write down the issues involved in multi threading. Also specify the solutions to those issues.

7 (a) Discuss briefly about reorder buffer and also explain how it addresses various types of dependences in a program.
(b) What is the need of register renaming? Explain with an example.

8 (a) Draw and explain the internal architecture of the Pentium 4 processor.
(b) Write a short note on MPI, open MP and PVM.

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ADVANCED COMPUTER ARCHITECTURE

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Answer any FIVE questions

All questions carry equal marks

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1 (a) Explain the program graph before and after grain packing with relevant example.
(b) Discuss about static multiprocessor scheduling.

2 (a) State and explain Amdahl's law for fixed work load.
(b) Explain VLIW architecture with a neat diagram.

3 Describe various cache memory address mapping techniques with their merits and demerits.

4 (a) Explain the 8×8 omega network unit with 2×2 switches and 4×4 switches.
(b) Draw and explain a two-stage & a three-stage butterfly network.

5 (a) Describe the three vector-access memory schemes with relevant diagrams.
(b) Write a short note on compound vector processing.

6 (a) What are distributed coherent caches? Write down its benefits.
(b) Explain briefly about processor consistency and release consistency.

7 (a) Differentiate between static scheduling and dynamic scheduling.
(b) Describe the loop unrolling technique and operand forwarding technique.

8 (a) Give the schematic block diagram of 2D torus network in Cray XT5 and explain.
(b) Write a short note on chapel.

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